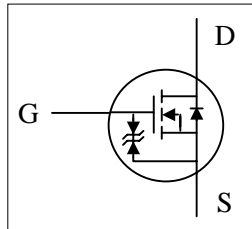




- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

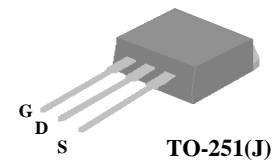
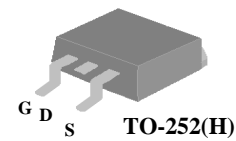


BV_{DSS}	500V
$R_{DS(ON)}$	1.6 Ω
I_D	5A

Description

AP05N50E series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance. The through-hole version (AP05N50EJ) are available for low-profile applications.



Absolute Maximum Ratings @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, V_{GS} @ 10V	5	A
I_{DM}	Pulsed Drain Current ¹	20	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	73.5	W
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	2	W
E_{AS}	Single Pulse Avalanche Energy ²	12.5	mJ
I_{AR}	Avalanche Current	5	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	1.7	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁴	62.5	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	110	$^\circ\text{C}/\text{W}$



Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	500	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =2A	-	-	1.6	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =2A	-	3.5	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =400V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±25V, V _{DS} =0V	-	-	±10	uA
Q _g	Total Gate Charge ³	I _D =1A	-	20	32	nC
Q _{gs}	Gate-Source Charge	V _{DS} =400V	-	4	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	8	-	nC
t _{d(on)}	Turn-on Delay Time ³	V _{DD} =250V	-	10	-	ns
t _r	Rise Time	I _D =1A	-	4	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	27	-	ns
t _f	Fall Time	V _{GS} =10V	-	18	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	775	1240	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	75	-	pF
C _{riss}	Reverse Transfer Capacitance	f=1.0MHz	-	10	-	pF
R _g	Gate Resistance	f=1.0MHz	-	3.5	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ³	I _S =2A, V _{GS} =0V	-	-	1.5	V
t _{rr}	Reverse Recovery Time ³	I _S =2A, V _{GS} =0V,	-	250	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	1.75	-	uC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Starting T_j=25°C , V_{DD}=50V , L=1mH , R_G=25Ω , I_{AS}=5A.
- 3.Pulse test
- 4.Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

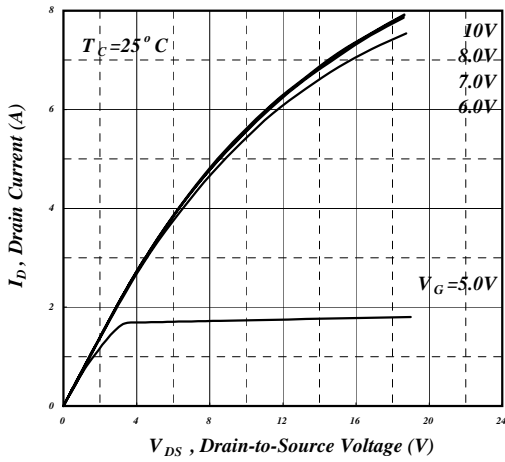


Fig 1. Typical Output Characteristics

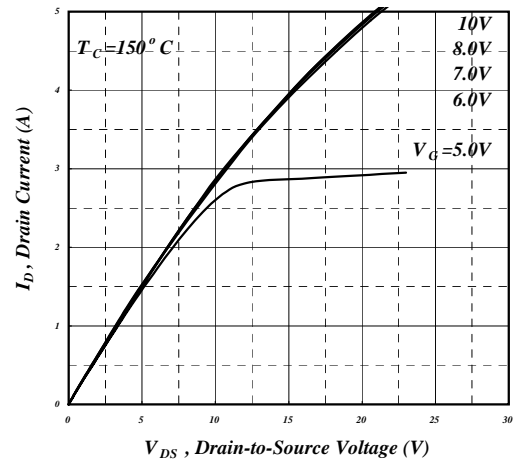


Fig 2. Typical Output Characteristics

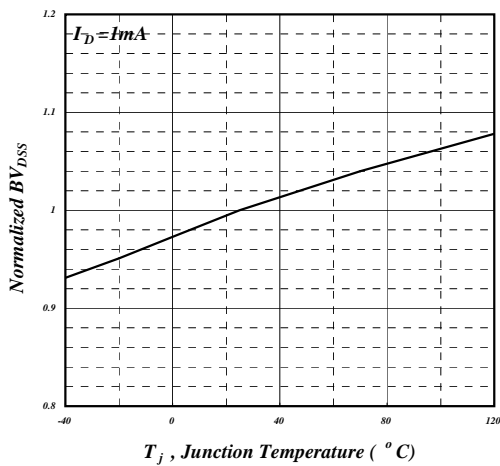


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

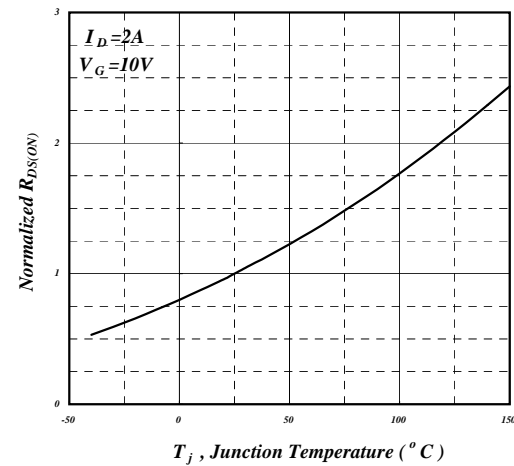


Fig 4. Normalized On-Resistance v.s. Junction Temperature

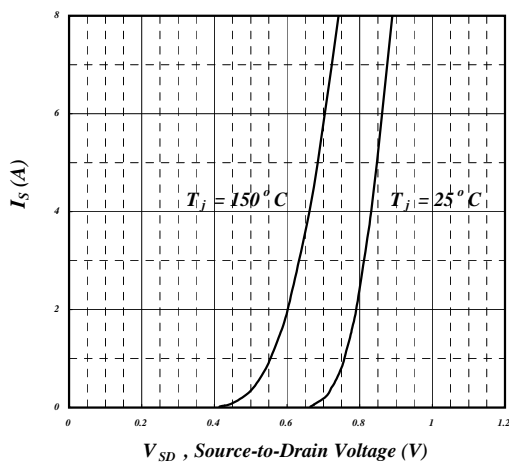


Fig 5. Forward Characteristic of Reverse Diode

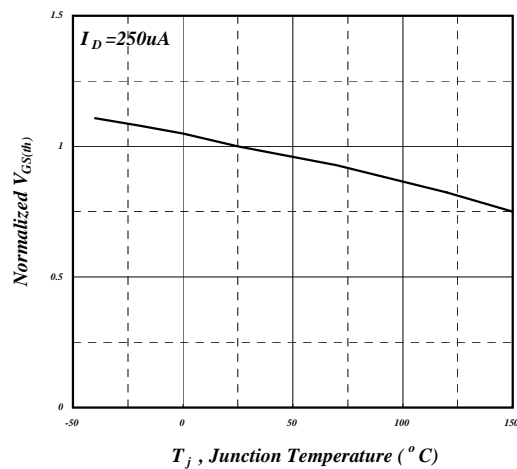


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



AP05N50EH/J-HF

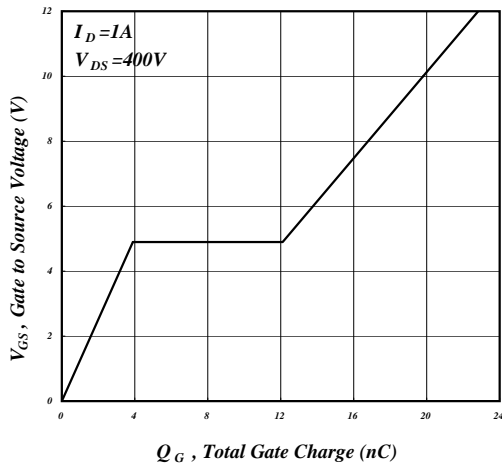


Fig 7. Gate Charge Characteristics

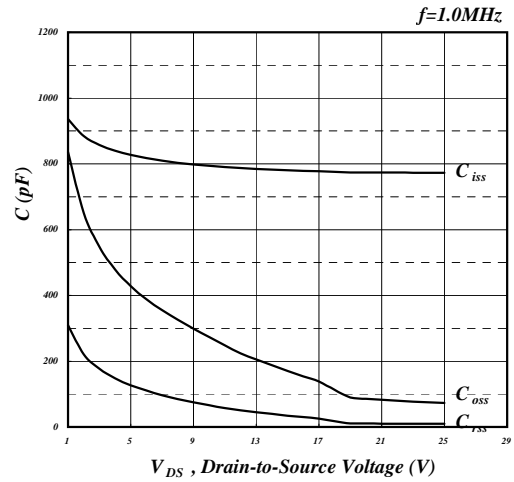


Fig 8. Typical Capacitance Characteristics

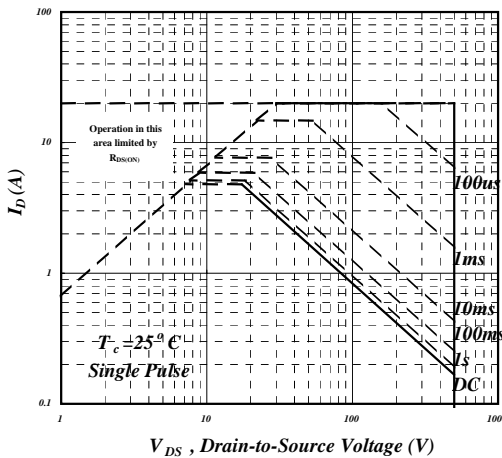


Fig 9. Maximum Safe Operating Area

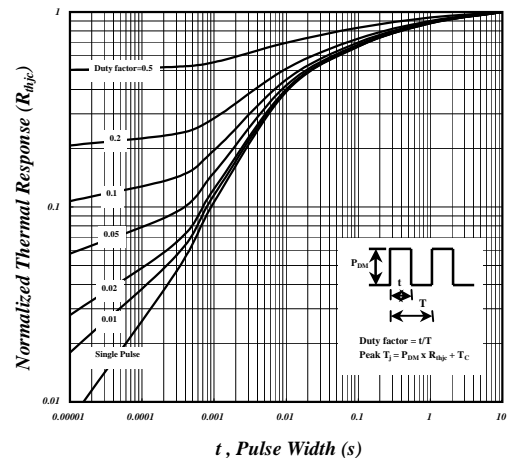


Fig 10. Effective Transient Thermal Impedance



Fig 11. Switching Time Waveform

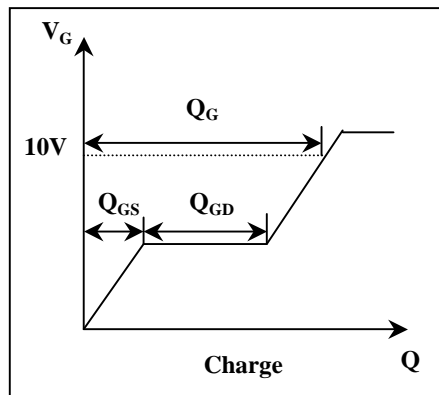
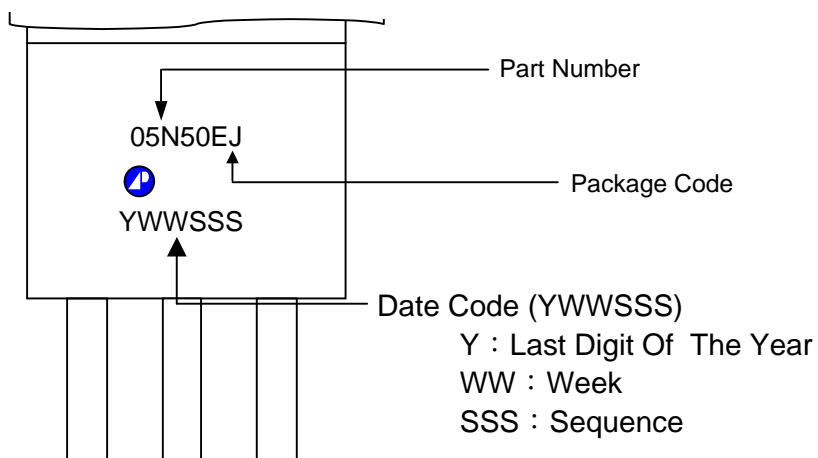


Fig 12. Gate Charge Waveform

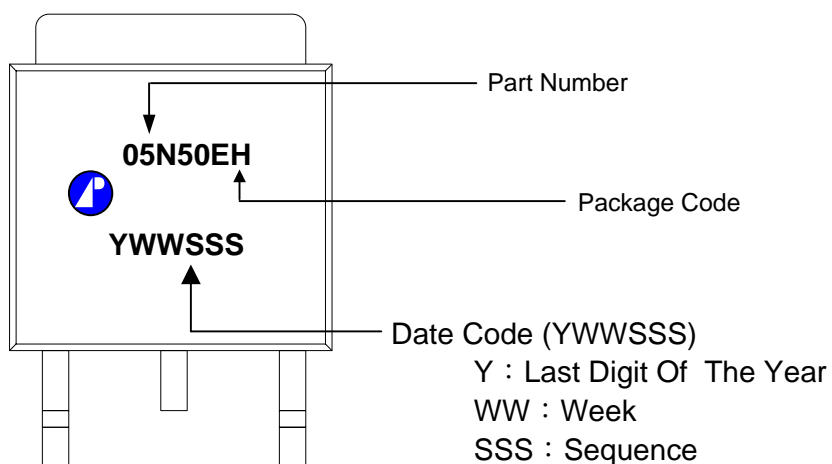


MARKING INFORMATION

TO-251



TO-252





Package Outline : TO-252



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A2	2.18	2.30	2.40
A3	0.40	0.50	0.65
B	0.40	0.70	1.00
B1	0.50	0.85	1.20
D	6.00	6.50	6.80
D1	4.80	5.35	5.90
E3	4.00 (ref.)		
F	2.00	2.63	3.05
F1	0.50	0.85	1.20
E1	5.00	5.70	6.30
E2	0.50	1.10	1.80
e	2.3 (ref)		
C	0.35	0.525	0.70
A1	0.00	—	0.25
B2	—	—	1.25
L	0.90	1.34	1.78



1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.
3. Thermal PAD, Body and Pin contour is for reference, it may has little difference by option.



TO-252 FOOTPRINT :

