

# AP10A250YT

**Halogen-Free Product**

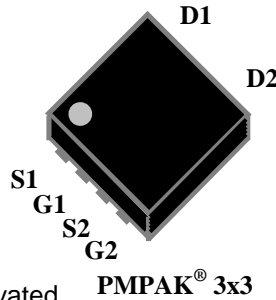


**Advanced Power  
Electronics Corp.**

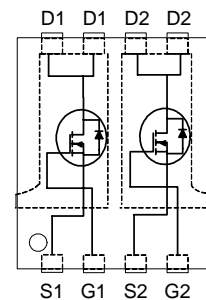
*DUAL N-CHANNEL ENHANCEMENT*

*MODE POWER MOSFET*

- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



$BV_{DSS}$	100V
$R_{DS(ON)}$	250m $\Omega$
$I_D^3$	2.1A



## Description

AP10A250 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device fo

The PMPAK<sup>®</sup> 3x3 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

## Absolute Maximum Ratings @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^\circ\text{C}$	Drain Current <sup>3</sup> , $V_{GS}$ @ 10V	2.1	A
$I_D @ T_A=70^\circ\text{C}$	Drain Current <sup>3</sup> , $V_{GS}$ @ 10V	1.7	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	10	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Rating	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	10	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	50	$^\circ\text{C}/\text{W}$



# AP10A250YT

## Electrical Characteristics @T<sub>j</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =2A	-	-	250	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =1A	-	-	500	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =2A	-	3	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =2A	-	5.5	8.8	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =50V	-	1.1	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =10V	-	1.8	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =50V	-	6	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =1A	-	7	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω	-	10	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	6	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	200	320	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =50V	-	25	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	20	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	2	4	Ω

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =1.9A, V <sub>GS</sub> =0V	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =2A, V <sub>GS</sub> =0V	-	30	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/μs	-	24	-	nC

### Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, t ≤ 10sec ; 90 °C/W on steady state.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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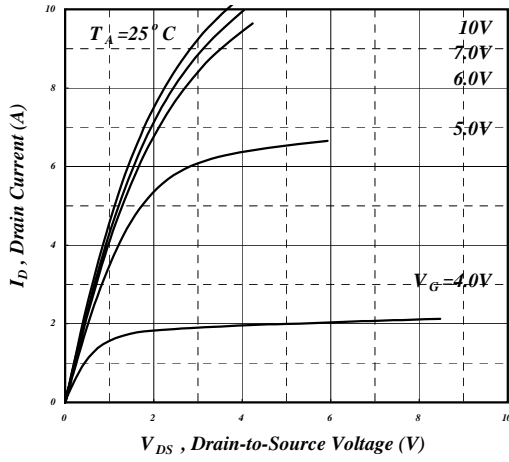


Fig 1. Typical Output Characteristics

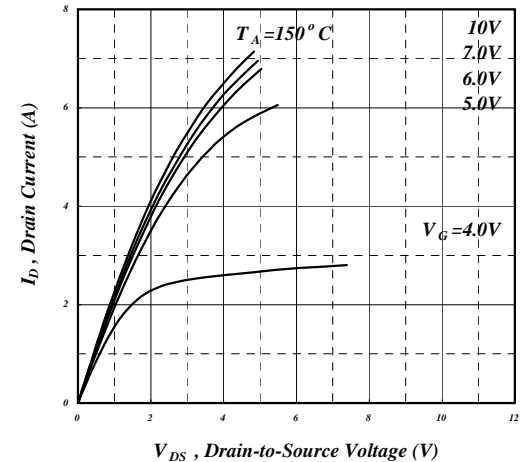


Fig 2. Typical Output Characteristics

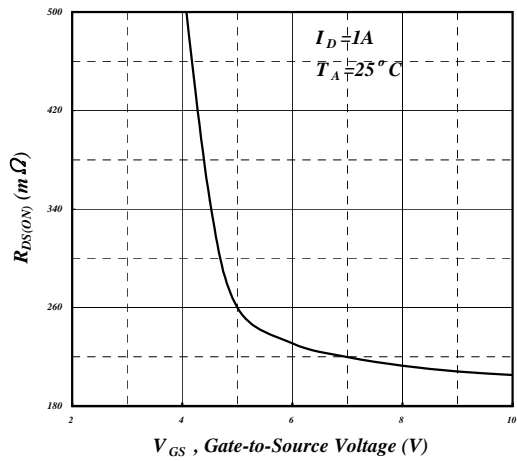


Fig 3. On-Resistance v.s. Gate Voltage

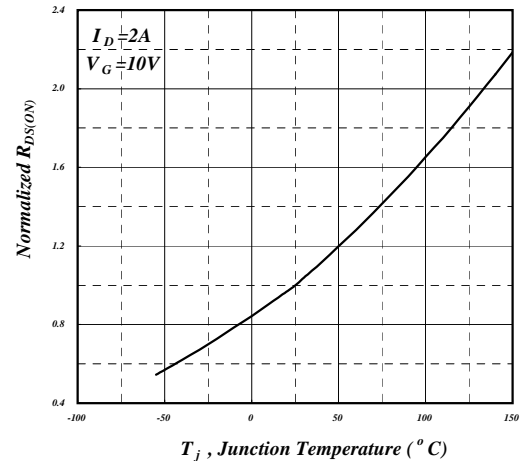


Fig 4. Normalized On-Resistance v.s. Junction Temperature

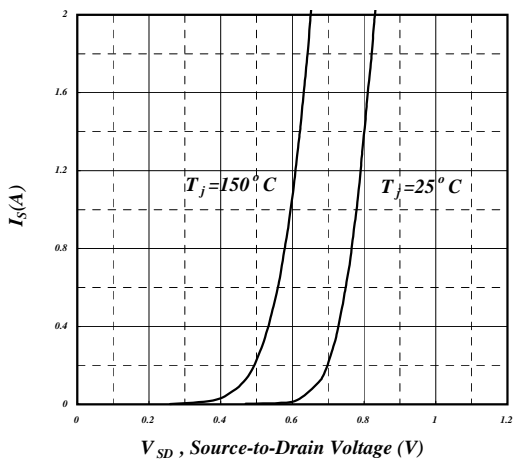


Fig 5. Forward Characteristic of Reverse Diode

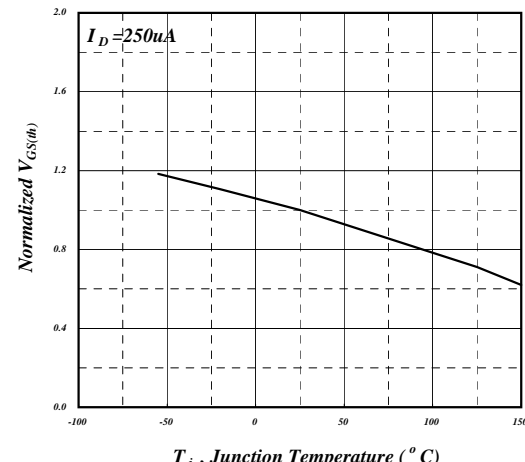


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

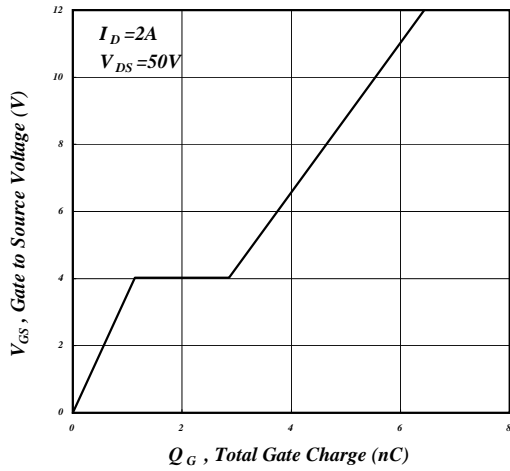


Fig 7. Gate Charge Characteristics

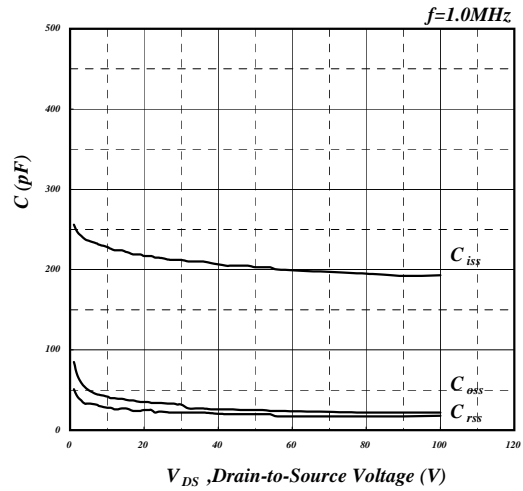


Fig 8. Typical Capacitance Characteristics

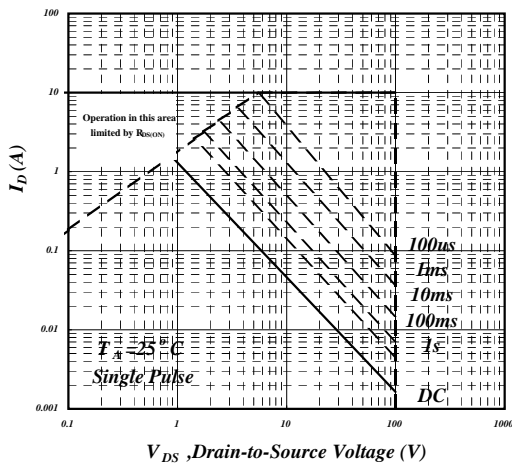


Fig 9. Maximum Safe Operating Area

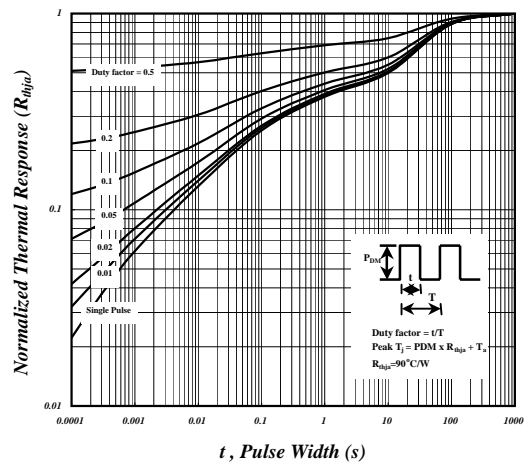


Fig 10. Effective Transient Thermal Impedance

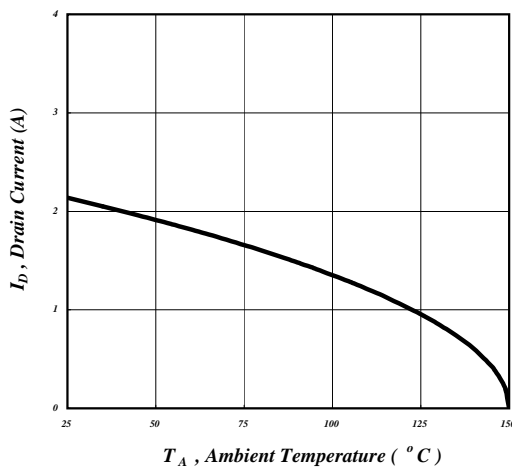


Fig 11. Drain Current v.s. Ambient Temperature

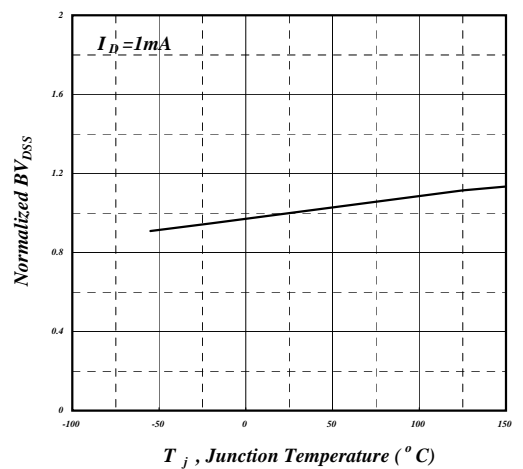
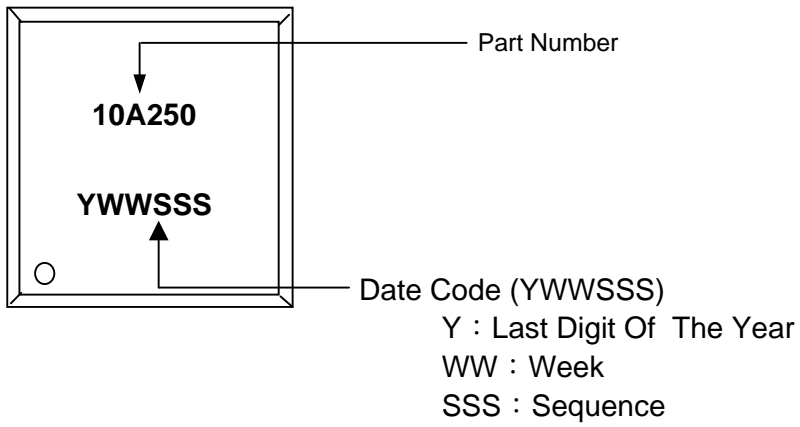


Fig 12. Normalized  $BV_{DSS}$  v.s. Junction Temperature



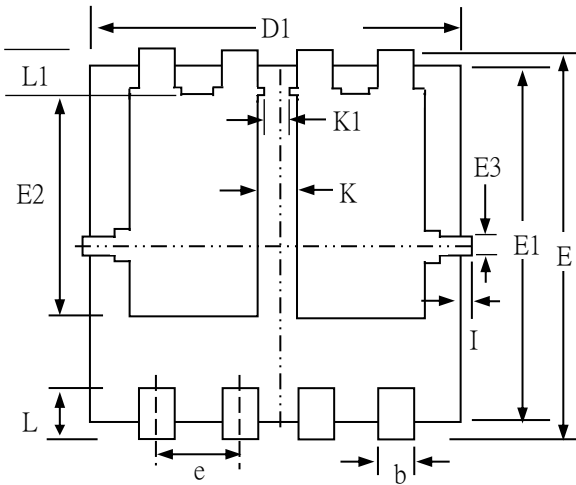
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**MARKING INFORMATION**

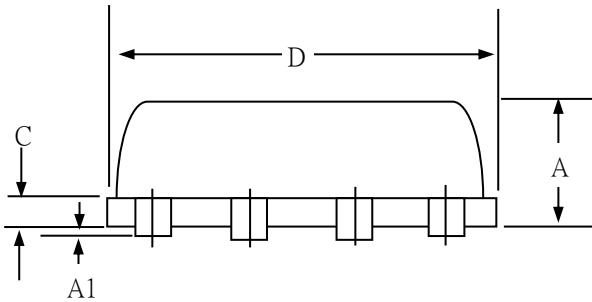




## Package Outline : PMPAK 3x3 (Dual Pad)



BACKSIDE VIEW

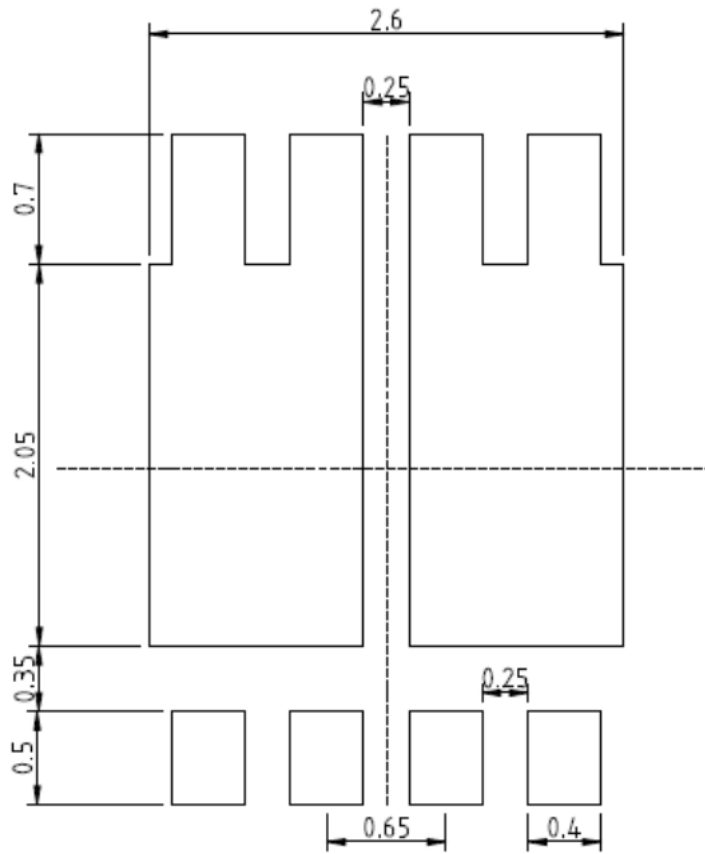


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.65	0.80	1.05
A1	-----	-----	0.15
b	0.20	0.35	0.50
C	0.10	0.15	0.25
D	2.85	3.30	3.60
D1	2.85	3.10	3.40
E	2.85	3.30	3.60
E1	2.85	3.10	3.40
E2	1.45	1.75	2.05
E3	0.10	0.20	0.30
e	0.65 (ref.)		
L	0.15	0.40	0.50
L1	0.15	0.50	0.70
K	0.20	0.38	0.65
K1	0.10	0.25	0.45
I	-----	-----	0.15

1. All Dimension Are In Millimeters.
2. Dimension Does Not Include Mold Protrusions.



**PMPAK3X3(Dual Pad) FOOTPRINT :**



UNIT: mm