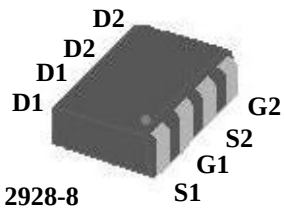
AP10C325Y

Halogen-Free Product

Advanced Power Electronics Corp.

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **HBM ESD 2kV**
- ▼ **Fast Switching Performance**
- ▼ **RoHS Compliant & Halogen-Free**

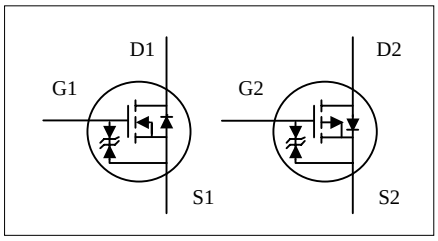


N-CH	BV_{DSS}	100V
	$R_{DS(ON)}$	325mΩ
	I_D[4]	2A
P-CH	BV_{DSS}	-100V
	$R_{DS(ON)}$	470mΩ
	I_D[4]	-1.5A

Description

AP10C325 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The 2928-8 J-lead package provides good on-resistance performance and space saving like TSOP-6.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	100	-100	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[4]	2	-1.5	A
I_{DM}	Pulsed Drain Current[1]	6	-6	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.38		W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	90	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=1mA	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=2A	-	-	325	mΩ
		V_{GS}=4.5V, I_D=2A	-	-	340	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.4	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=2A	-	7.5	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±30	uA
Q_g	Total Gate Charge	I_D=2A	-	6.5	10.4	nC
Q_{gs}	Gate-Source Charge	V_{DS}=50V	-	1.4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	1.3	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V	-	15	-	ns
t_r	Rise Time	I_D=1A	-	12	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	63	-	ns
t_f	Fall Time	V_{GS}=10V	-	27	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	310	496	pF
C_{oss}	Output Capacitance	V_{DS}=50V	-	21	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	14	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time	I_S=2A, V_{GS}=0V	-	18	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	13	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-1mA	-100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-1.5A	-	-	470	mΩ
		V_{GS}=-4.5V, I_D=-0.75A	-	-	510	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-2.5	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-1.5A	-	5	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-80V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±30	uA
Q_g	Total Gate Charge	I_D=-1.5A	-	14	22.4	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-50V	-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-10V	-	2.5	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-50V	-	15	-	ns
t_r	Rise Time	I_D=-1A	-	11	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	110	-	ns
t_f	Fall Time	V_{GS}=-10V	-	25	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	680	1088	pF
C_{oss}	Output Capacitance	V_{DS}=-50V	-	30	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	24	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward On Voltage[2]	I_S=-1A, V_{GS}=0V	-	-	-1.3	V
t_{rr}	Reverse Recovery Time	I_S=-1.5A, V_{GS}=0V	-	21	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	23	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 210°C/W at steady state.

4.Ensure that the junction temperature does not exceed $T_{Jmax.}$.

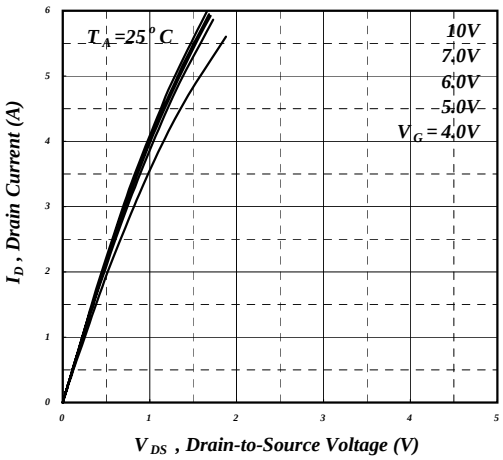


Fig 1. Typical Output Characteristics

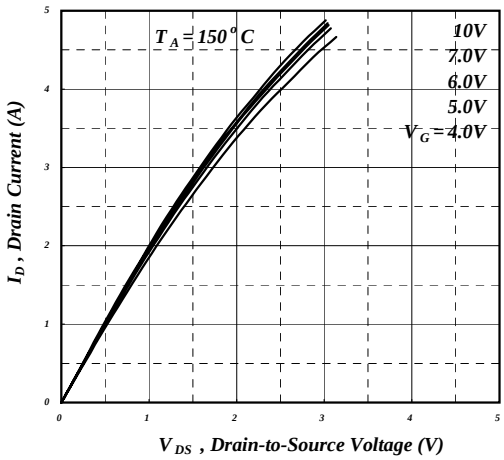


Fig 2. Typical Output Characteristics

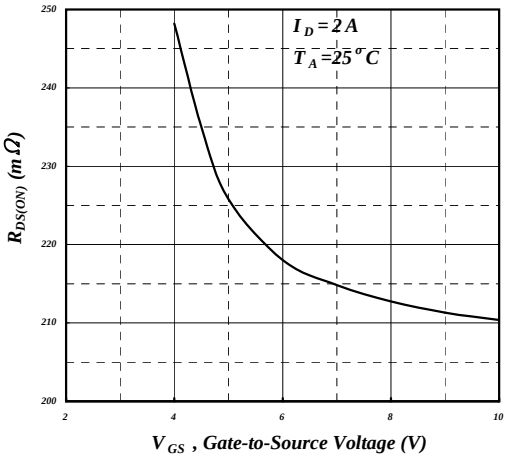


Fig 3. On-Resistance v.s. Gate Voltage

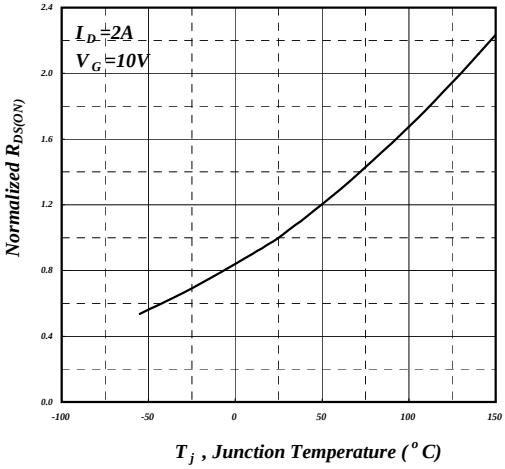


Fig 4. Normalized On-Resistance v.s. Junction Temperature

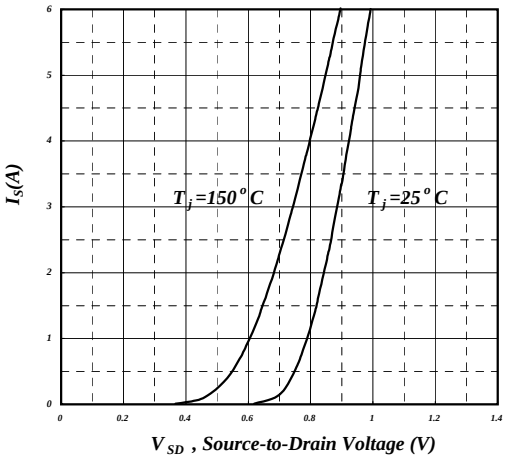


Fig 5. Forward Characteristic of Reverse Diode

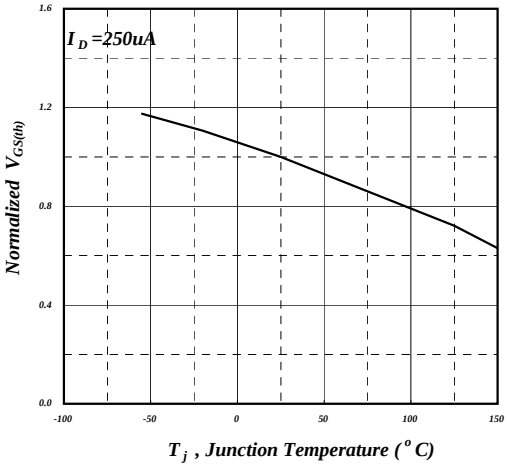


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

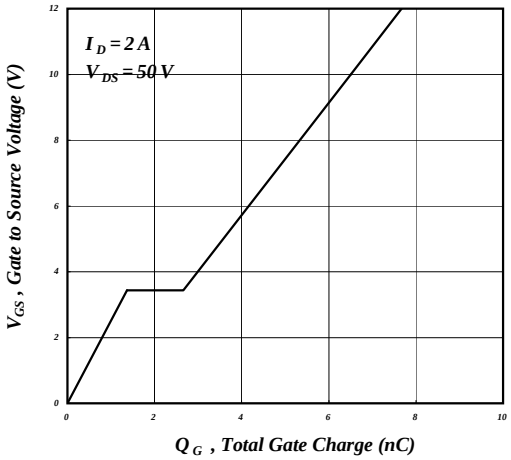


Fig 7. Gate Charge Characteristics

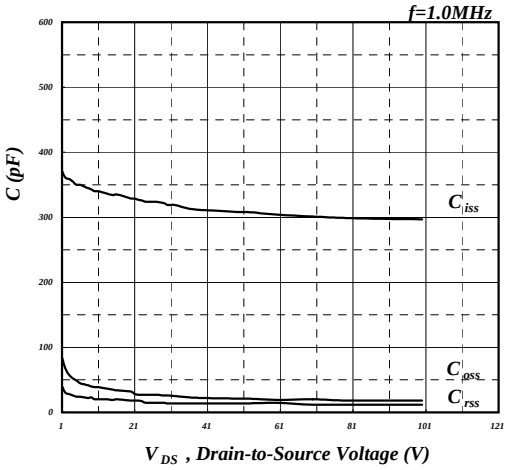


Fig 8. Typical Capacitance Characteristics

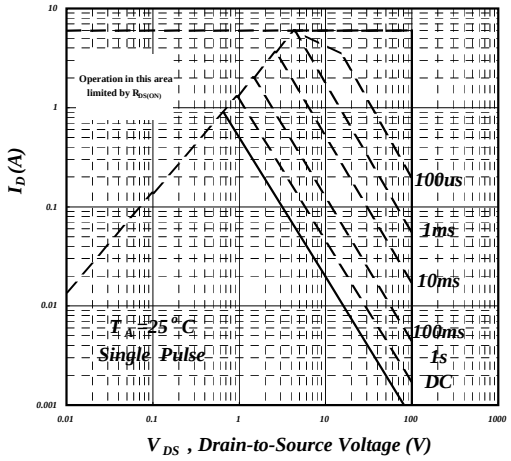


Fig 9. Maximum Safe Operating Area

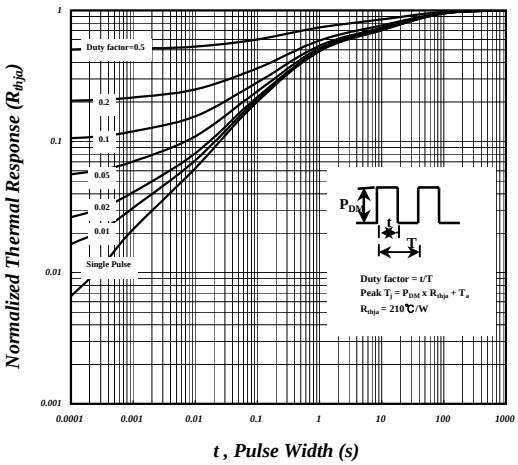


Fig 10. Effective Transient Thermal Impedance

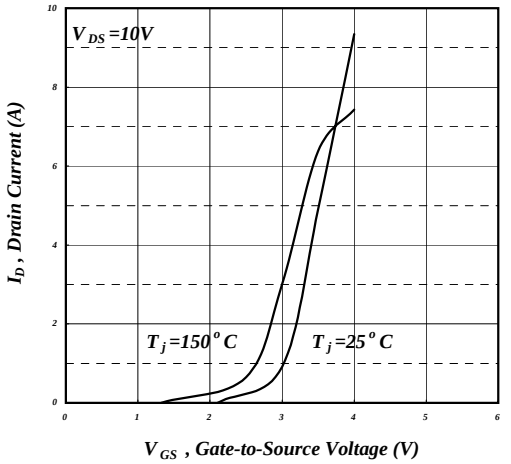


Fig 11. Transfer Characteristics

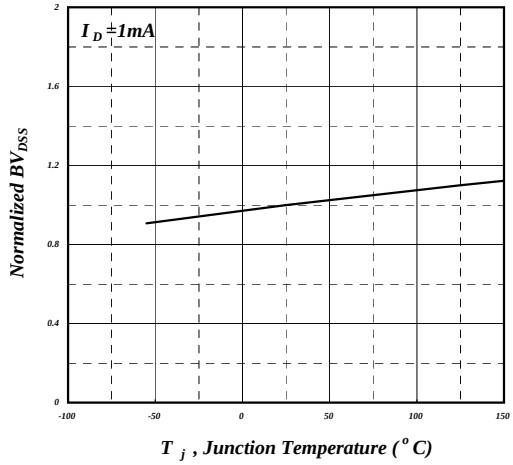


Fig 12. Normalized BV_{DSS} v.s. Junction

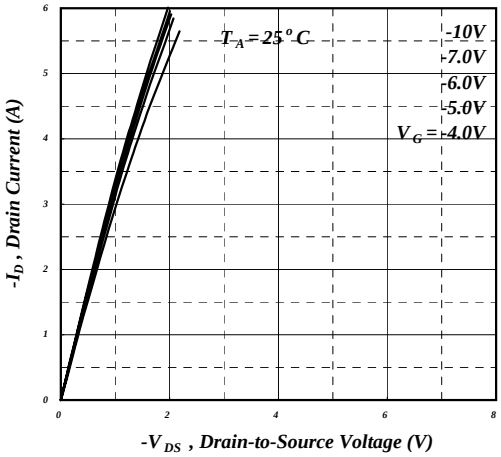


Fig 1. Typical Output Characteristics

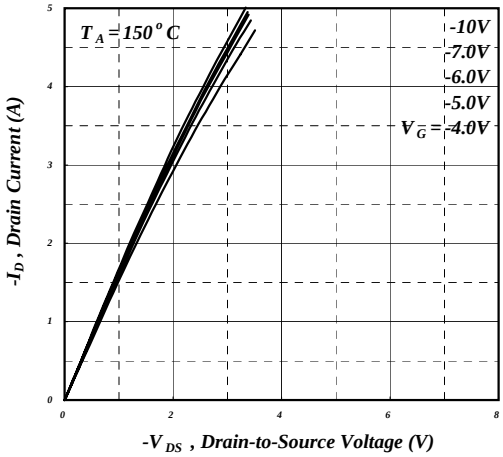


Fig 2. Typical Output Characteristics

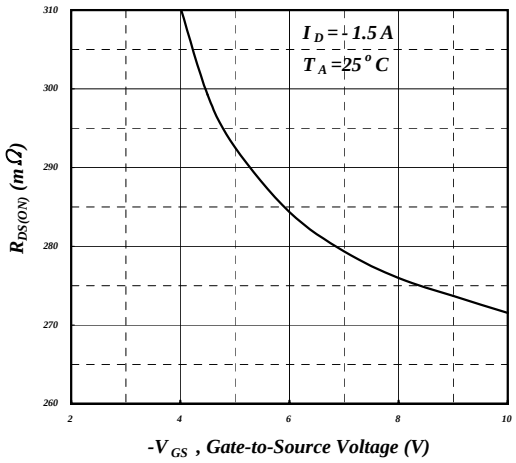


Fig 3. On-Resistance v.s. Gate Voltage

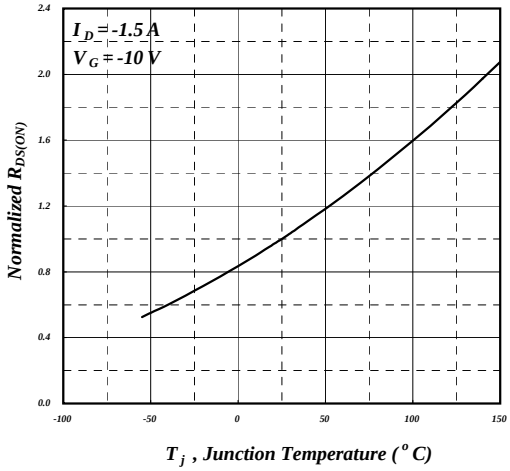


Fig 4. Normalized On-Resistance v.s. Junction Temperature

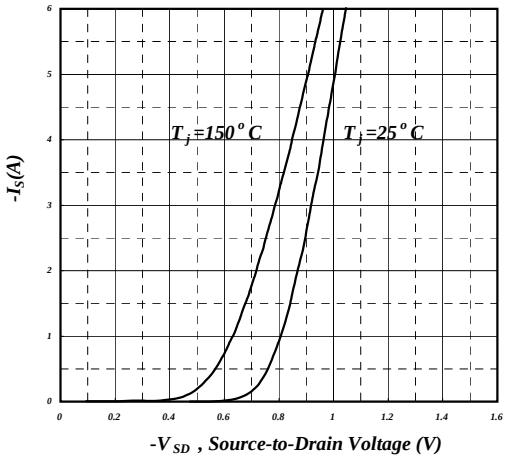


Fig 5. Forward Characteristic of Reverse Diode

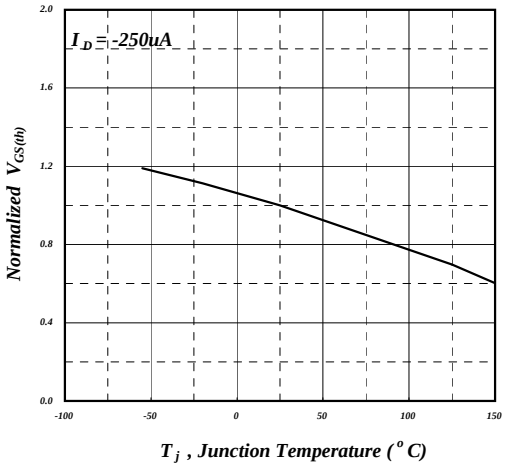


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

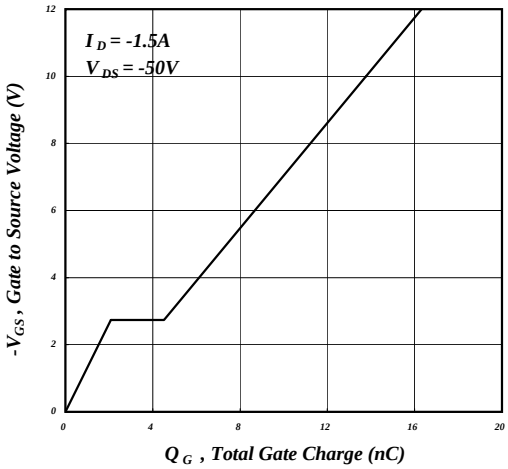


Fig 7. Gate Charge Characteristics

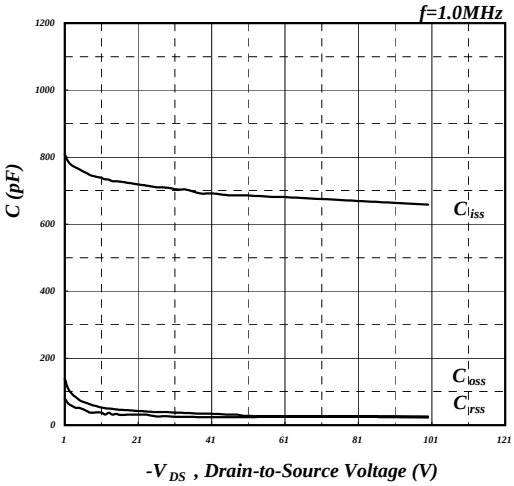


Fig 8. Typical Capacitance Characteristics

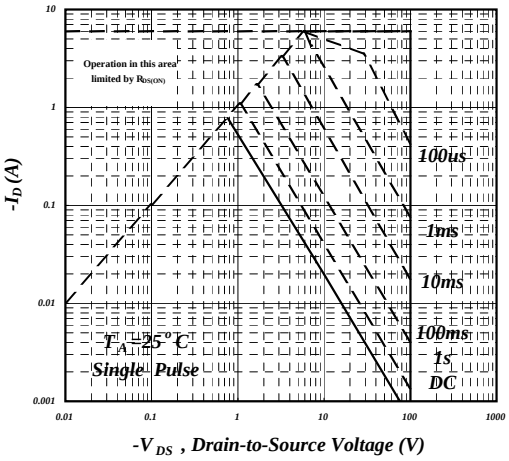


Fig 9. Maximum Safe Operating Area

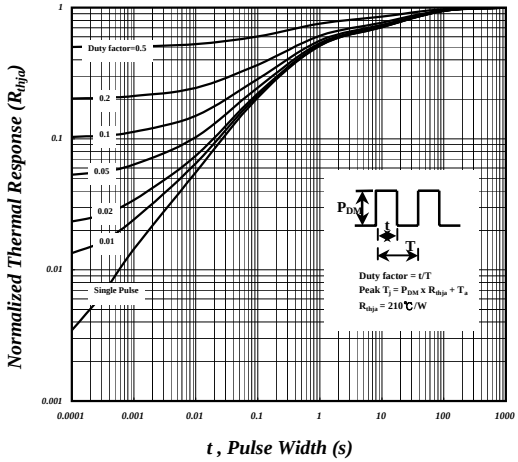


Fig 10. Effective Transient Thermal Impedance

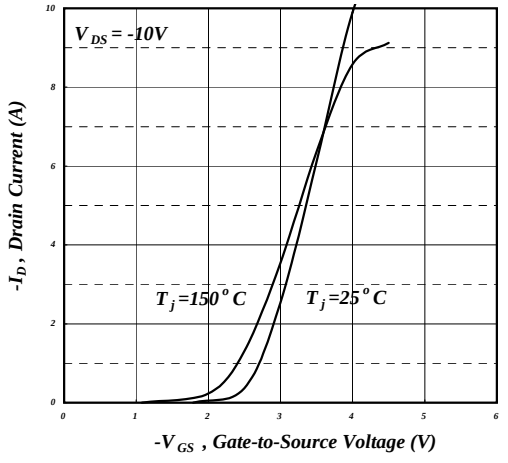


Fig 11. Transfer Characteristics

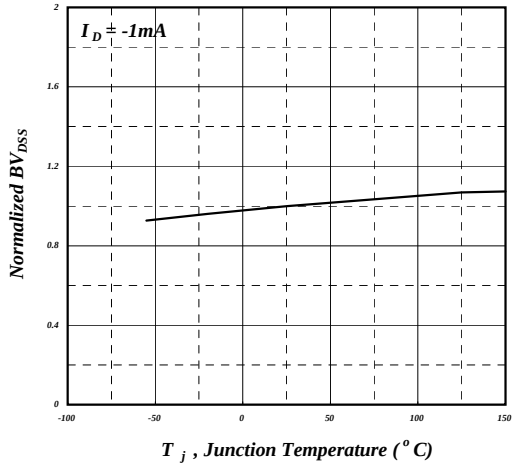
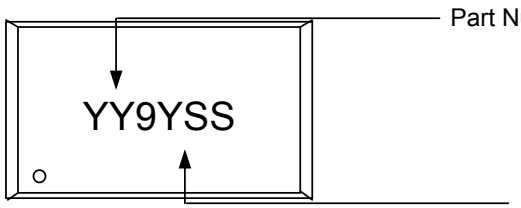


Fig 12. Normalized BV_{DSS} v.s. Junction

MARKING INFORMATION



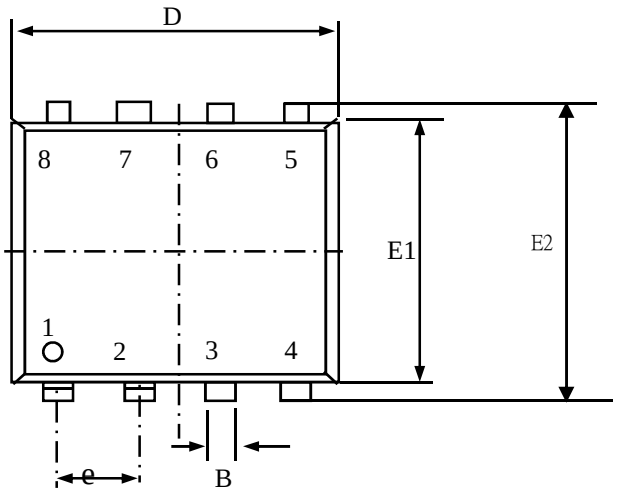
Part Number : YY9

Date Code (YSS)

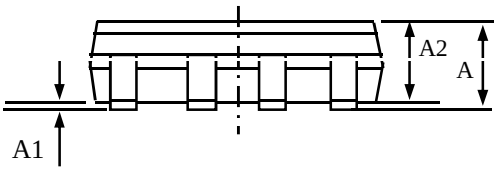
Y：Last Digit Of The Year

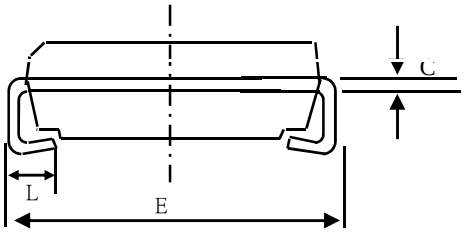
SS：Sequence

Package Outline : 2928-8



SYMBOLS	Millimeters		
	MIN	NOM	MAX
E	2.50	----	3.00
E1	2.30	2.40	2.50
E2	2.65	2.85	3.05
L	0.30	0.45	0.60
A	0.93	---	1.10
A1	0.01	---	0.10
A2	0.92	---	1.00
D	2.95	3.05	3.10
B	0.25	0.32	0.40
C	0.10	0.15	0.20
e	0.65BSC		





Note: 1.All Dimensions Are in Millimeters.

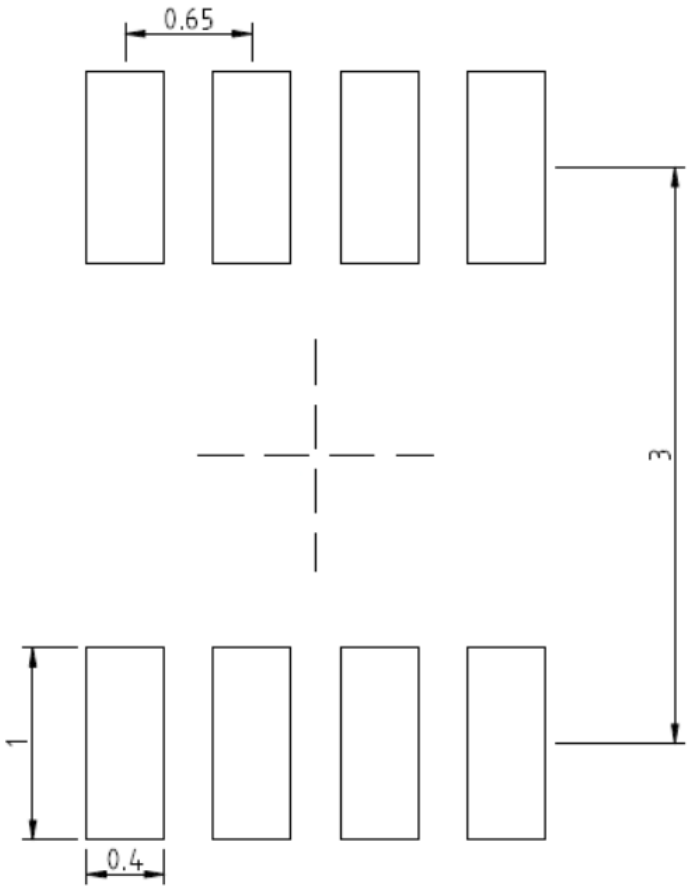
2.Package Body Sizes Exclude Mold Flash, Protrusion or Gate Burrs.
Mold Flash, Protrusion or Gate Burrs Shall Not Exceed 0.10mm Per Side.

3.Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.

4.The Package Top May Be Smaller Than The Package Bottom.

5. Dimension"b" Does Not Include Dambar Protrusion. Allowable Damber Protrusion Shall Be 0.08mm Total In Excess Of "b" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.

2928-8 FOOTPRINT：



UNIT: mm