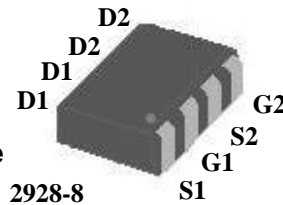




- ▼ Simple Drive Requirement
- ▼ Low Gate Charge
- ▼ Fast Switching Performance
- ▼ RoHS Compliant & Halogen-Free

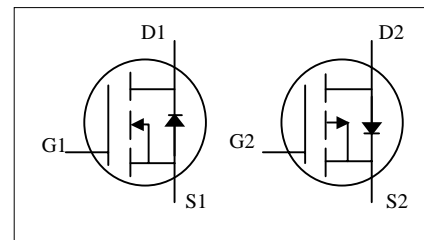


N-CH	BV_{DSS}	30V
	$R_{DS(ON)}$	20m Ω
	I_D	6.5A
P-CH	BV_{DSS}	-30V
	$R_{DS(ON)}$	45m Ω
	I_D	-4.6A

Description

AP3700 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The 2928-8 J-lead package provides good on-resistance performance and space saving like TSOP-6.



Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	6.5	-4.6	A
$I_D @ T_A=70^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	5.2	-3.6	A
I_{DM}	Pulsed Drain Current ¹	20	-20	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	1.38		W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	90	$^\circ\text{C}/\text{W}$



AP3700Y

N-CH Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =6A	-	-	20	mΩ
		V _{GS} =4.5V, I _D =4A	-	-	35	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =1mA	1.5	-	2.2	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =6A	-	18	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	μA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =4A	-	5	8	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	1.8	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	1.8	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	7	-	ns
t _r	Rise Time	I _D =1A	-	10	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω	-	19	-	ns
t _f	Fall Time	V _{GS} =10V	-	4	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	550	880	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	90	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	60	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =1.2A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =6A, V _{GS} =0V	-	10	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	3	-	nC

**P-CH Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-4A$	-	-	45	m Ω
		$V_{GS}=-4.5V, I_D=-3A$	-	-	85	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-2	V
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-4A$	-	7.5	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V$	-	-	-10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_D=-3A$	-	6	9.6	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-15V$	-	1.8	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	2.1	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=-15V$	-	10	-	ns
t_r	Rise Time	$I_D=-1A$	-	11	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=6\Omega$	-	30	-	ns
t_f	Fall Time	$V_{GS}=-10V$	-	14	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	610	980	pF
C_{oss}	Output Capacitance	$V_{DS}=-15V$	-	100	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	70	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=-1.2A, V_{GS}=0V$	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	$I_S=-4A, V_{GS}=0V$	-	12	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	4	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 210°C/W at steady state.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



N-Channel

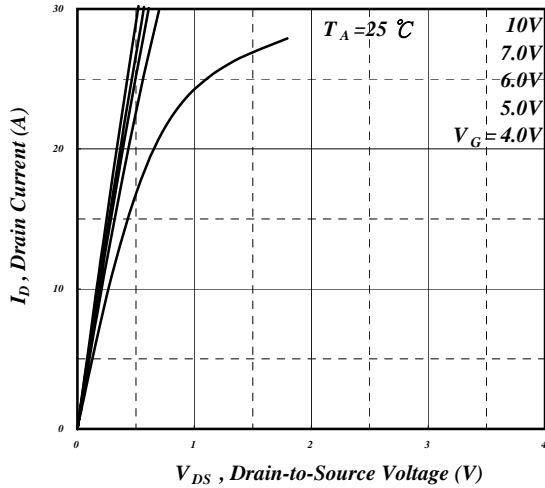


Fig 1. Typical Output Characteristics

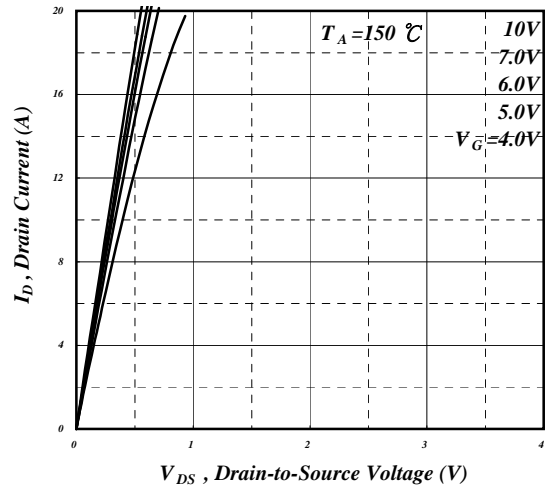


Fig 2. Typical Output Characteristics

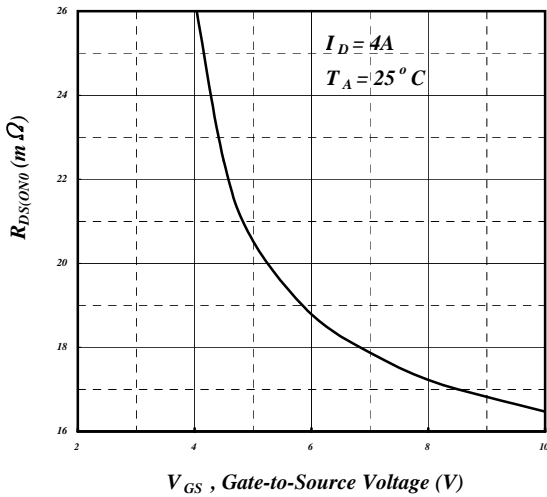


Fig 3. On-Resistance v.s. Gate Voltage

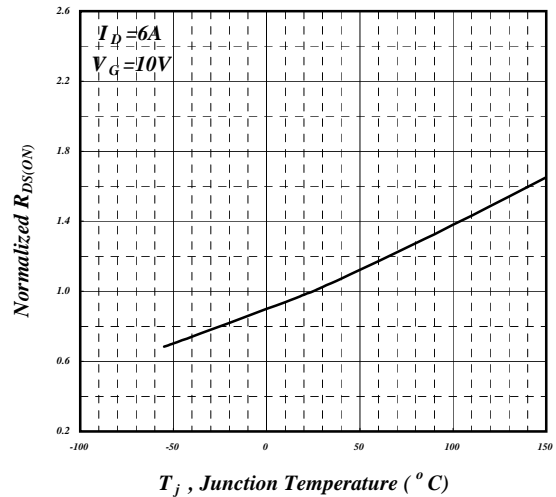


Fig 4. Normalized On-Resistance v.s. Junction Temperature

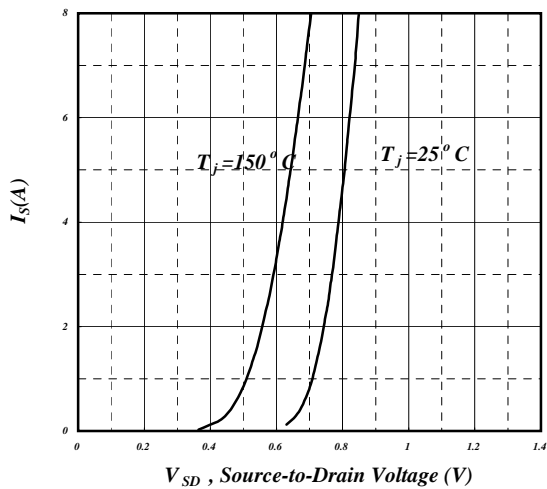


Fig 5. Forward Characteristic of Reverse Diode

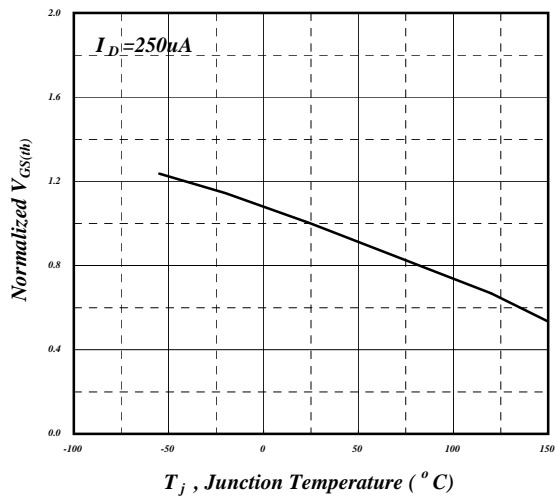


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

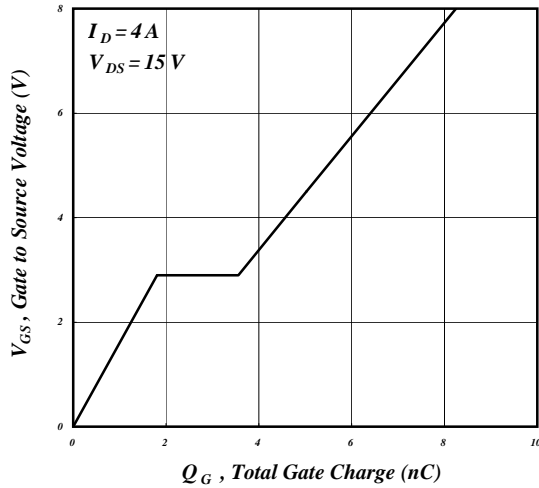


Fig 7. Gate Charge Characteristics

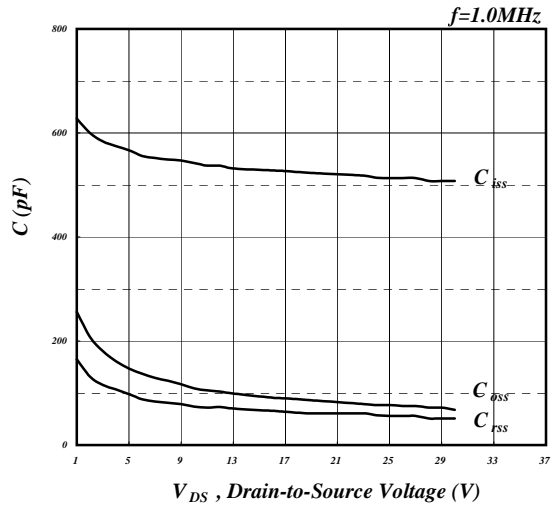


Fig 8. Typical Capacitance Characteristics

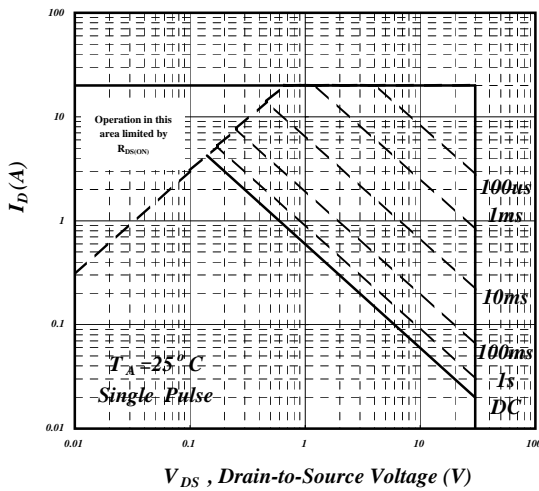


Fig 9. Maximum Safe Operating Area

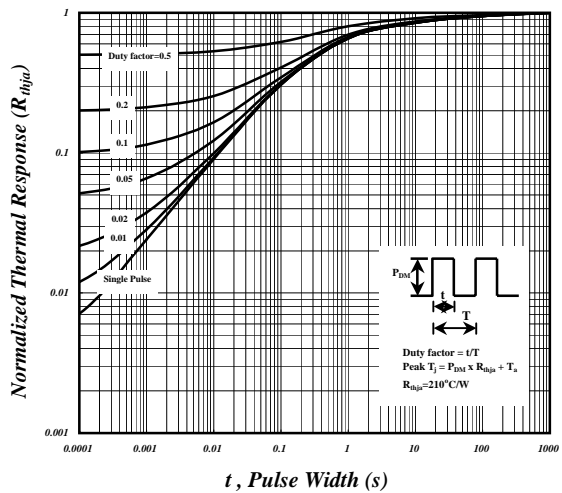


Fig 10. Effective Transient Thermal Impedance

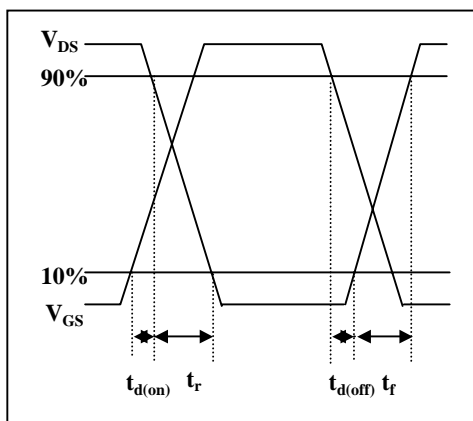


Fig 11. Switching Time Waveform

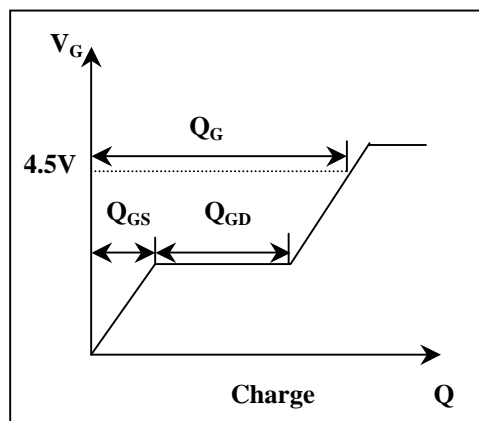


Fig 12. Gate Charge Waveform



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N-Channel

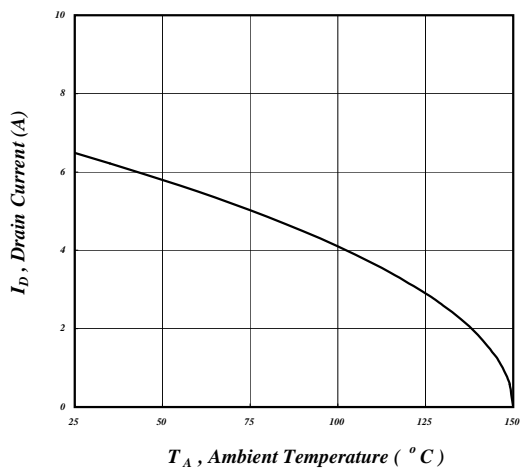


Fig 13. Drain Current v.s. Ambient Temperature

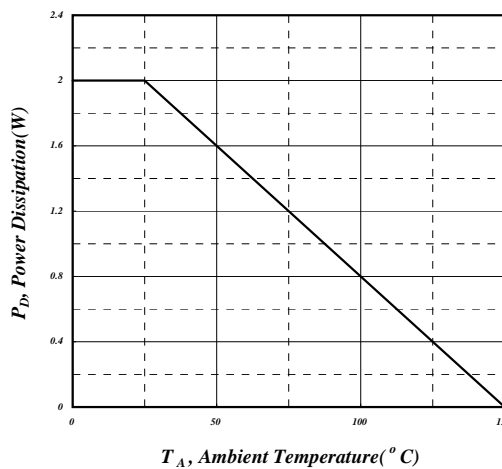


Fig 14. Total Power Dissipation

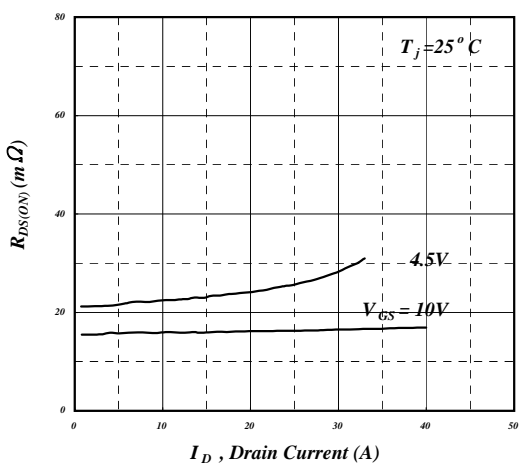


Fig 15. Typ. Drain-Source on State Resistance

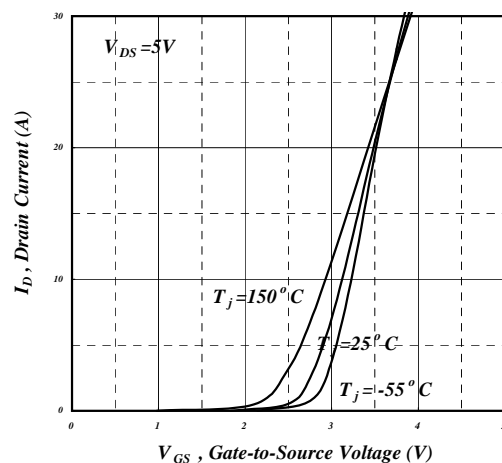


Fig 16. Transfer Characteristics



P-Channel

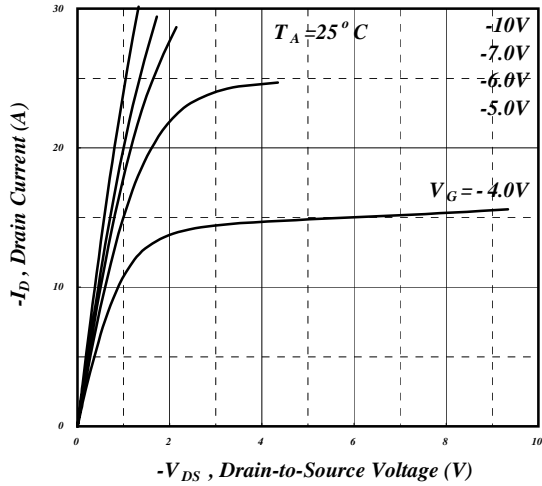


Fig 1. Typical Output Characteristics

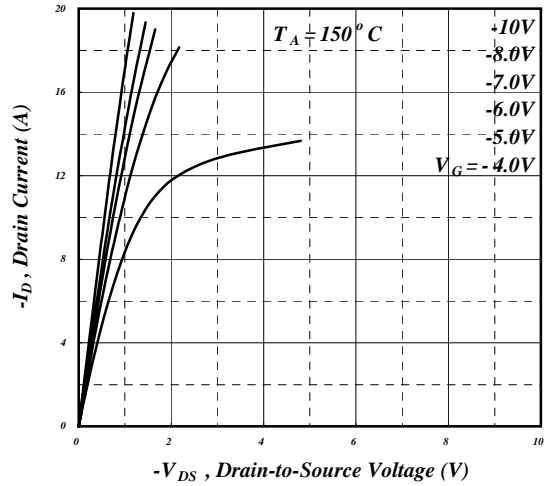


Fig 2. Typical Output Characteristics

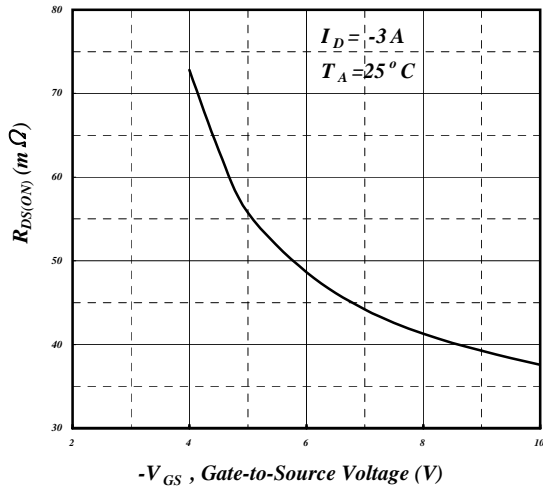


Fig 3. On-Resistance v.s. Gate Voltage

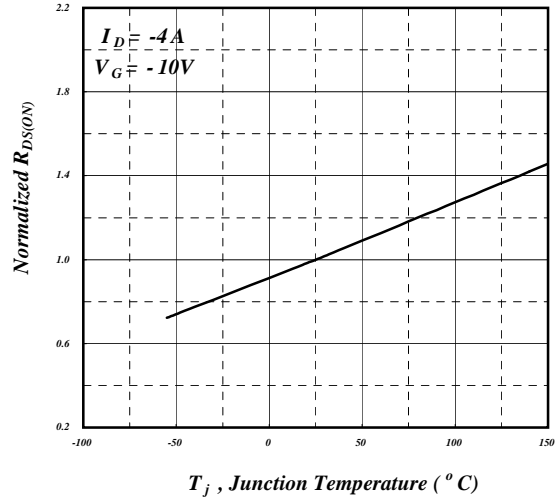


Fig 4. Normalized On-Resistance v.s. Junction Temperature

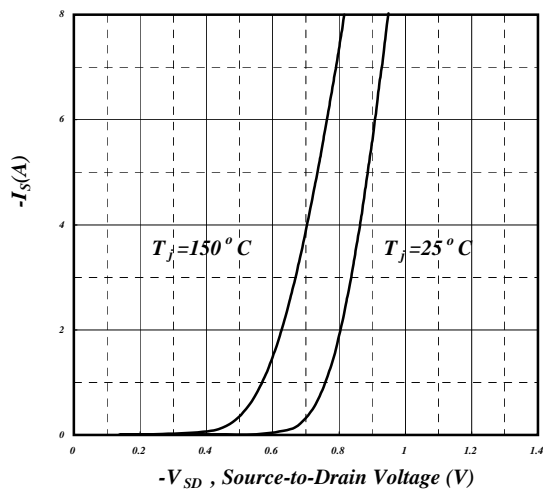


Fig 5. Forward Characteristic of Reverse Diode

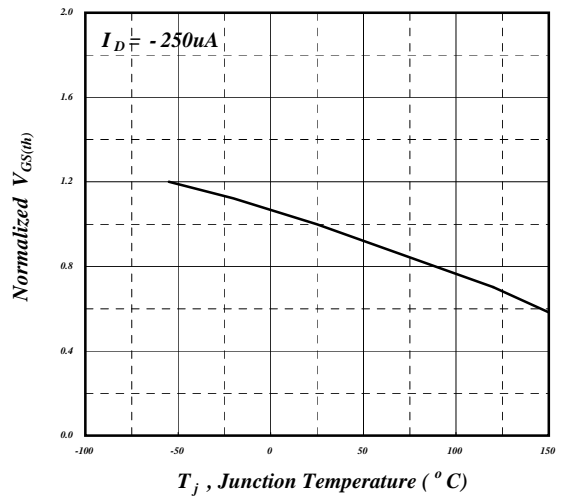


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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P-Channel

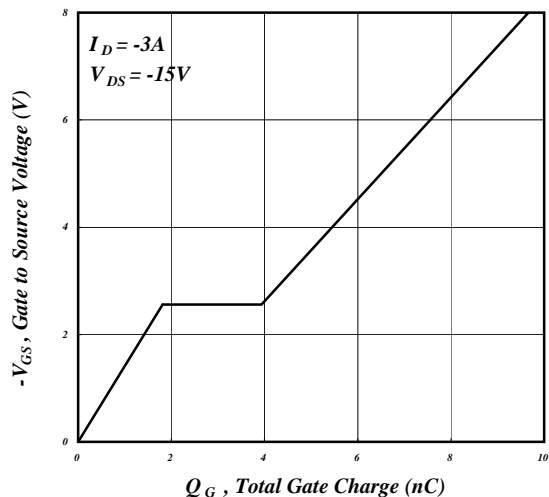


Fig 7. Gate Charge Characteristics

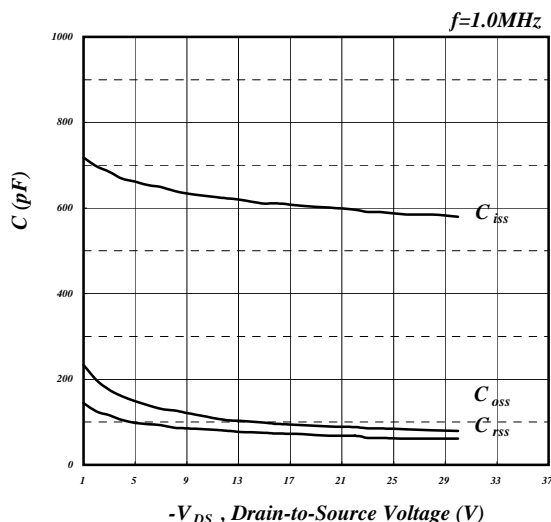


Fig 8. Typical Capacitance Characteristics

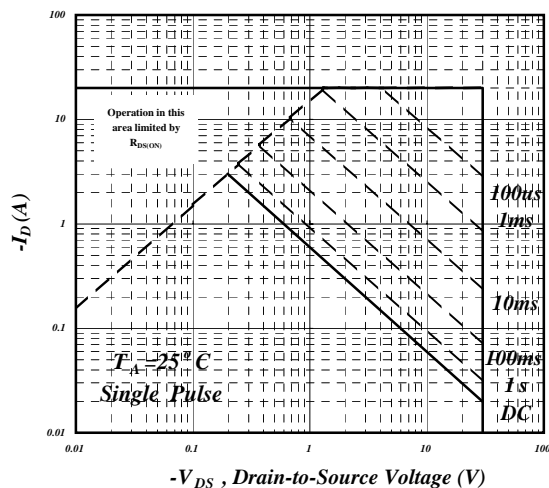


Fig 9. Maximum Safe Operating Area

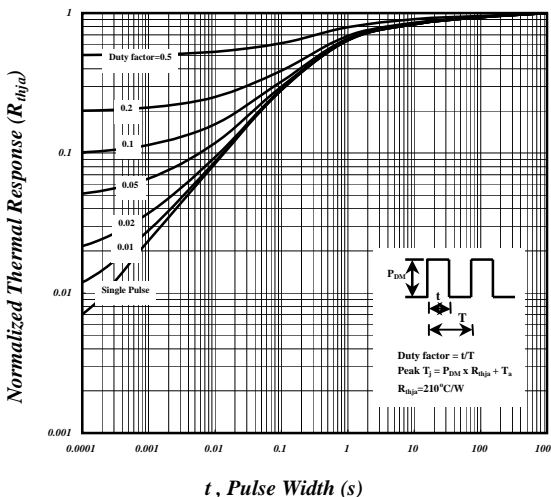


Fig 10. Effective Transient Thermal Impedance

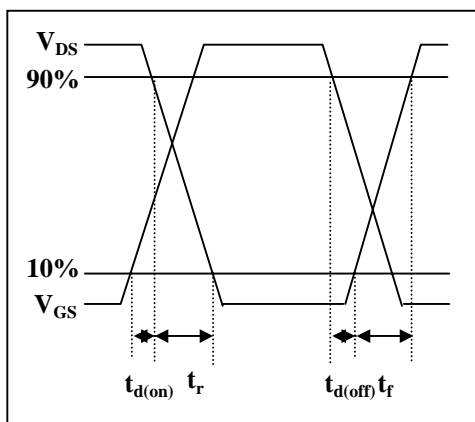


Fig 11. Switching Time Waveform

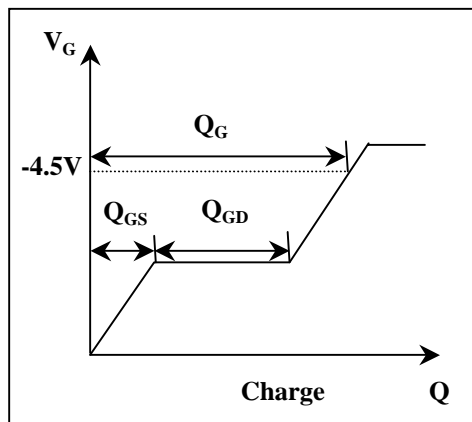


Fig 12. Gate Charge Waveform



P-Channel

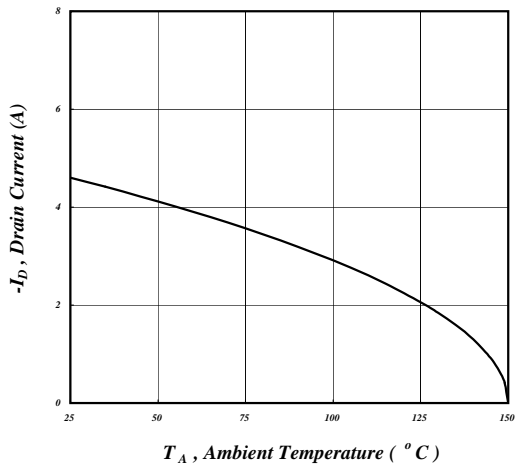


Fig 13. Drain Current v.s. Ambient Temperature

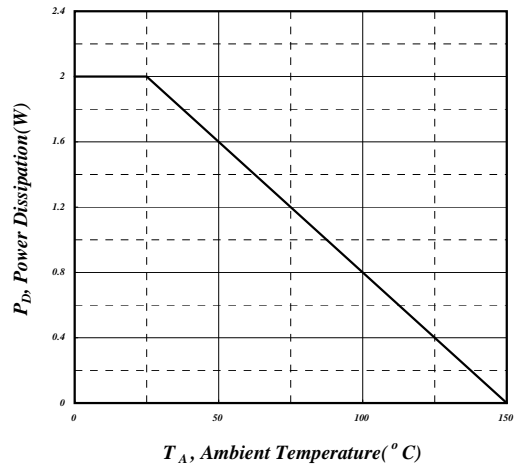


Fig 14. Total Power Dissipation

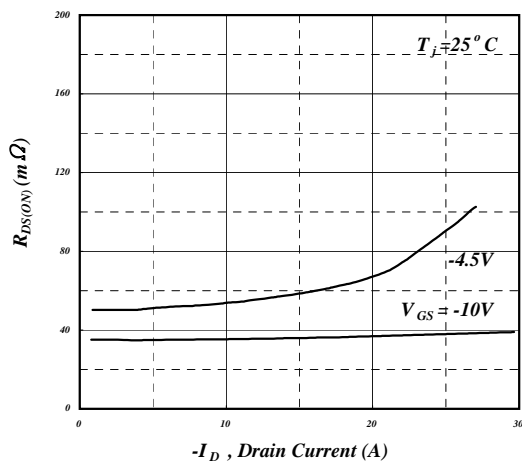


Fig 15. Typ. Drain-Source on State Resistance

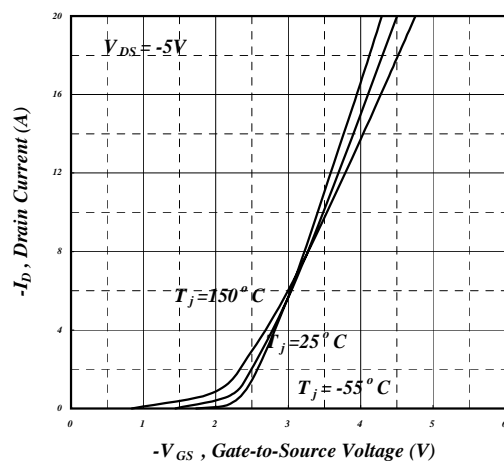
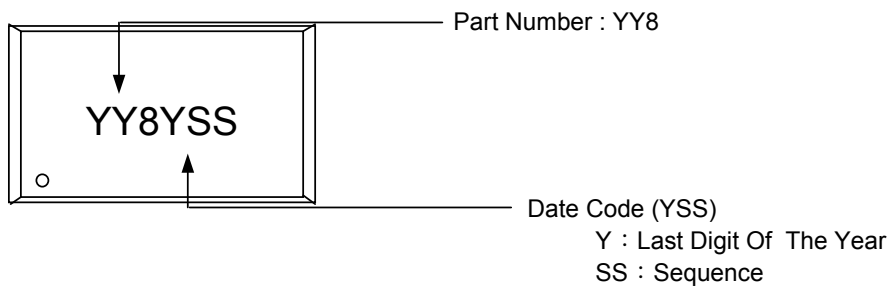


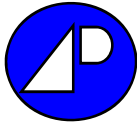
Fig 16. Transfer Characteristics



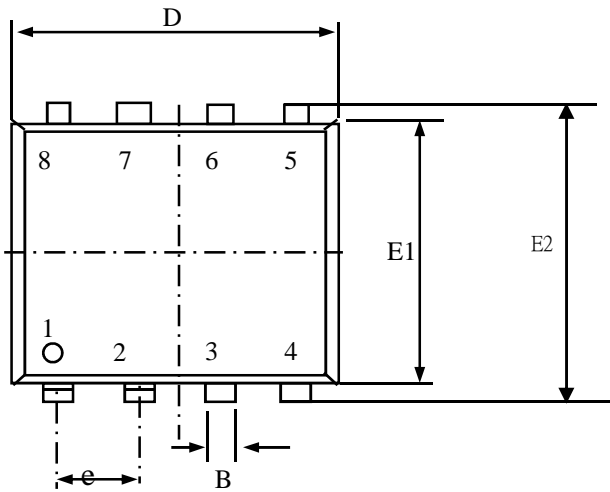
AP3700Y

MARKING INFORMATION

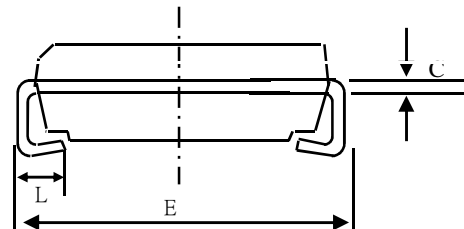
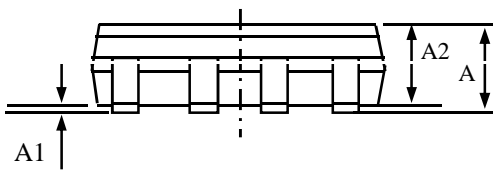




Package Outline : 2928-8



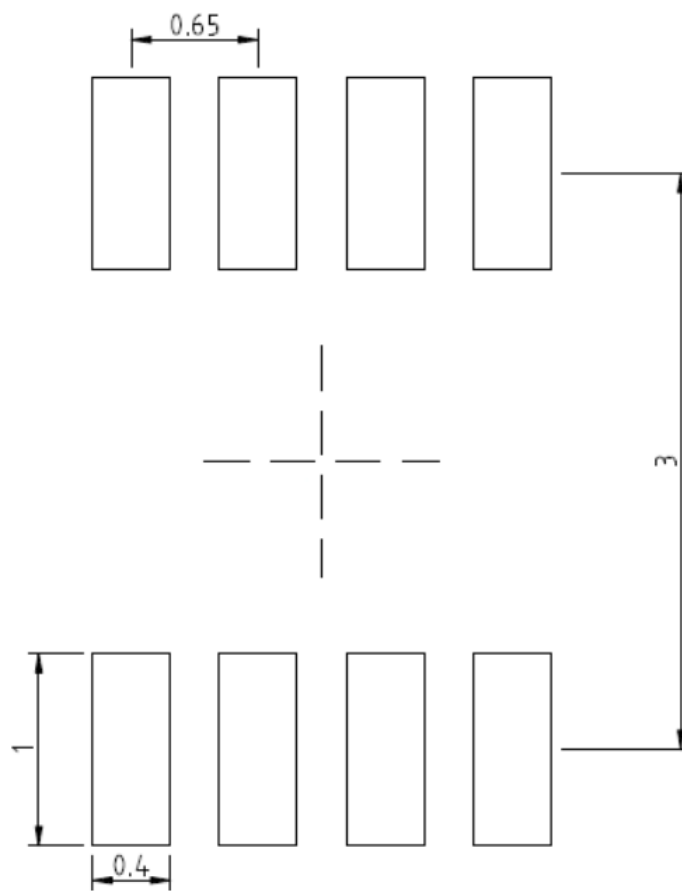
SYMBOLS	Millimeters		
	MIN	NOM	MAX
E	2.50	----	3.00
E1	2.30	2.40	2.50
E2	2.65	2.85	3.05
L	0.30	0.45	0.60
A	0.93	---	1.10
A1	0.01	---	0.10
A2	0.92	---	1.00
D	2.95	3.05	3.10
B	0.25	0.32	0.40
C	0.10	0.15	0.20
e	0.65BSC		



- Note:
1. All Dimensions Are in Millimeters.
 2. Package Body Sizes Exclude Mold Flash, Protrusion or Gate Burrs.
Mold Flash, Protrusion or Gate Burrs Shall Not Exceed 0.10mm Per Side.
 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
 4. The Package Top May Be Smaller Than The Package Bottom.
 5. Dimension "b" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08mm Total In Excess Of "b" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.



2928-8 FOOTPRINT :



UNIT: mm