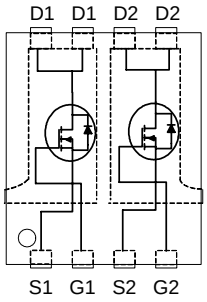
# AP3A010MT

**Halogen-Free Product**

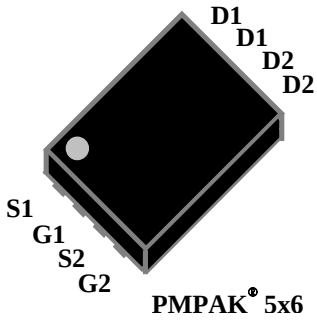
**Advanced Power Electronics Corp.**

*DUAL N-CHANNEL ENHANCEMENT MODE POWER MOSFET*

- ▼ **Simple Drive Requirement**
- ▼ **Fast Switching Characteristic**
- ▼ **RoHS Compliant & Halogen-Free**




| | |
|---|---|
| $BV_{DSS}$ | 30V |
| $R_{DS(ON)}$ | 10.5mΩ |




## Description

AP3A010 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device fo

PMPAK ® 5x6 dual pad provide superior thermal performance and is design for surface mount applications.

## Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 30 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_C$=25℃ | Drain Current, $V_{GS}$ @ 10V[4] | 34 | A |
| $I_D$@$T_A$=25℃ | Drain Current, $V_{GS}$ @ 10V[3,4] | 14.6 | A |
| $I_D$@$T_A$=70℃ | Drain Current, $V_{GS}$ @ 10V[3,4] | 11.7 | A |
| $I_{DM}$ | Pulsed Drain Current[1] | 80 | A |
| $P_D$@$T_A$=25℃ | Total Power Dissipation | 3.57 | W |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |

## Thermal Data

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| Rthj-c | Maximum Thermal Resistance, Junction-case | 6 | ℃/W |
| Rthj-a | Maximum Thermal Resistance, Junction-ambient[3] | 35 | ℃/W |

## Electrical Characteristics@$T_j$=25°C(unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250uA | 30 | - | - | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V, $I_D$=14A | - | - | 10.5 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=10A | - | - | 17 | mΩ |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250yA | 1 | - | 3 | V |
| $g_{fs}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=14A | - | 34 | - | S |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=24V, $V_{GS}$=0V | - | - | 25 | uA |
| $I_{GSS}$ | Gate-Source Leakage | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| $Q_g$ | Total Gate Charge | $I_D$=10A | - | 16 | 25.6 | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{DS}$=15V | - | 5 | - | nC |
| $Q_{gd}$ | Gate-Drain ("Miller") Charge | $V_{GS}$=4.5V | - | 5.5 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DS}$=15V | - | 9 | - | ns |
| $t_r$ | Rise Time | $I_D$=1A | - | 9 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G$=3.3Ω | - | 30 | - | ns |
| $t_f$ | Fall Time | $V_{GS}$=10V | - | 7 | - | ns |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V | - | 1830 | 2928 | pF |
| $C_{oss}$ | Output Capacitance | $V_{DS}$=15V | - | 180 | - | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | f=1.0MHz | - | 150 | - | pF |
| $R_g$ | Gate Resistance | f=1.0MHz | - | 1 | 2 | Ω |

## Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Forward On Voltage[2] | $I_S$=2.9A, $V_{GS}$=0V | - | - | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_S$=14A, $V_{GS}$=0V, | - | 10 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | dI/dt=100A/μs | - | 2.5 | - | nC |

### Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 $in^2$ copper pad of FR4 board, t ≤10sec ; 85 ℃/W on steady state.

4.Package limitation current is 20A .

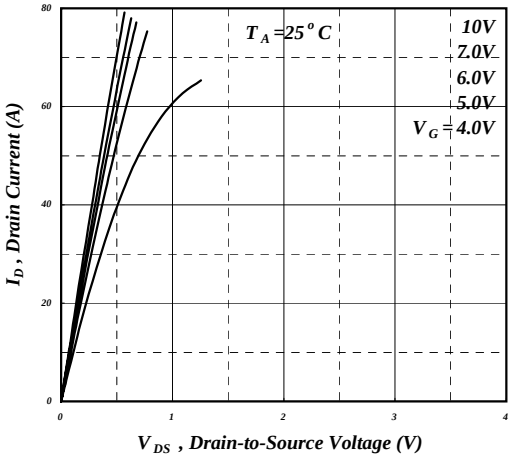



**Fig 1. Typical Output Characteristics**

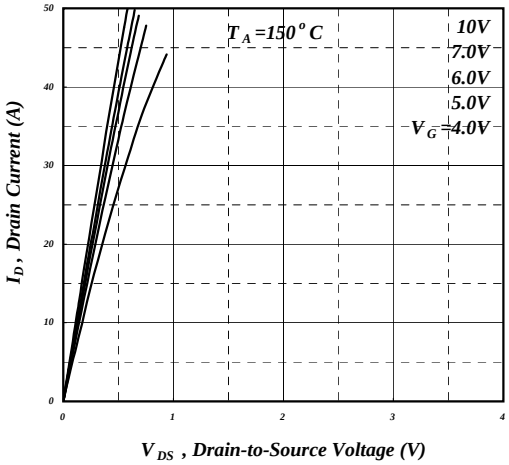



**Fig 2. Typical Output Characteristics**

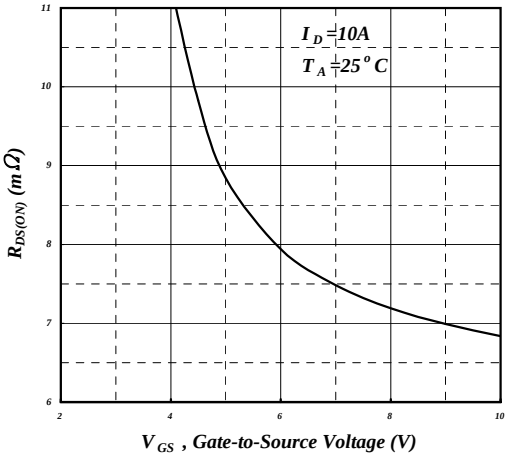



**Fig 3. On-Resistance v.s. Gate Voltage**

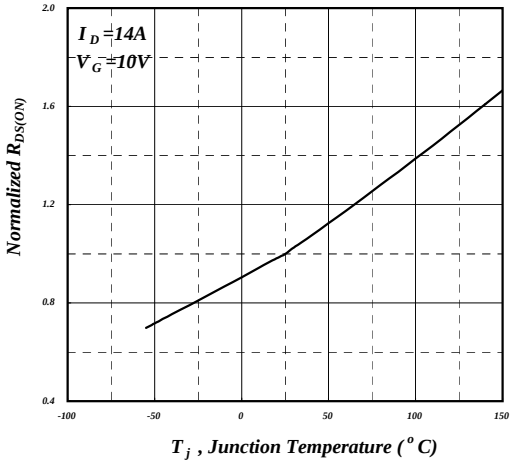



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

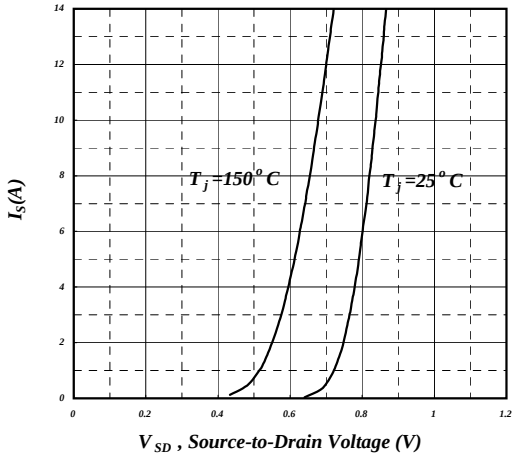



**Fig 5. Forward Characteristic of Reverse Diode**

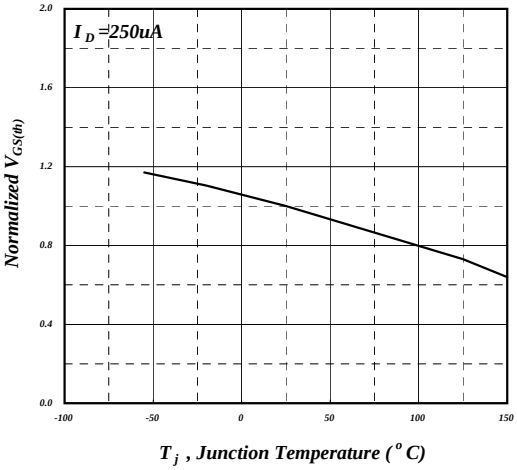



**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**

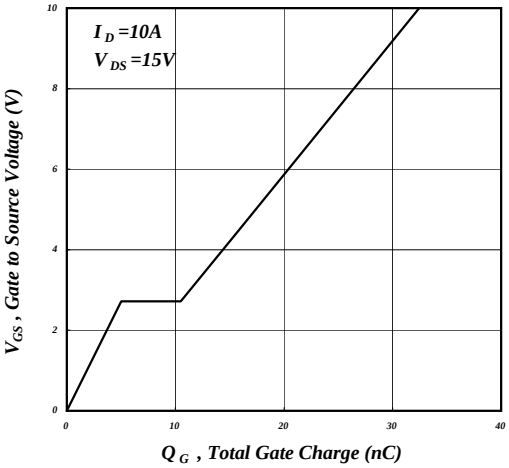



Fig 7. Gate Charge Characteristics

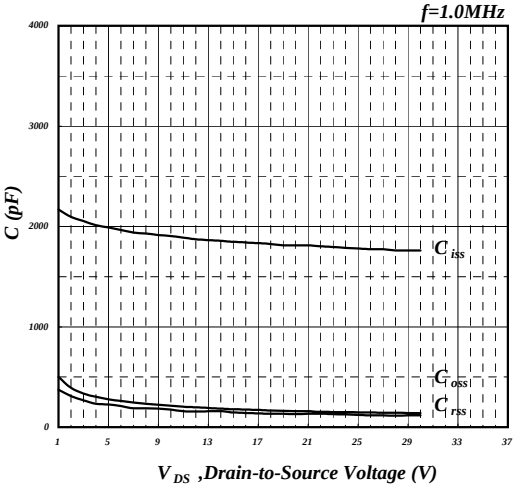



Fig 8. Typical Capacitance Characteristics

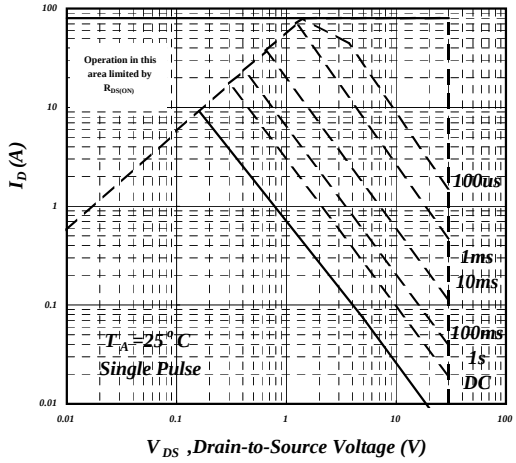



Fig 9. Maximum Safe Operating Area

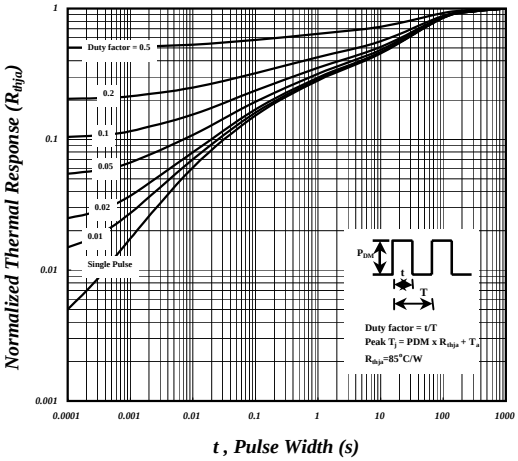



Fig 10. Effective Transient Thermal Impedance

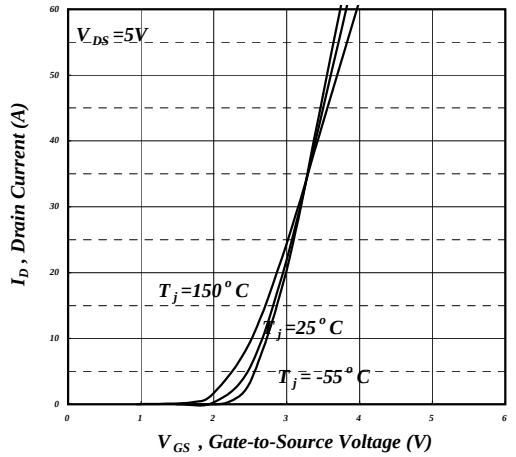



Fig 11. Transfer Characteristics

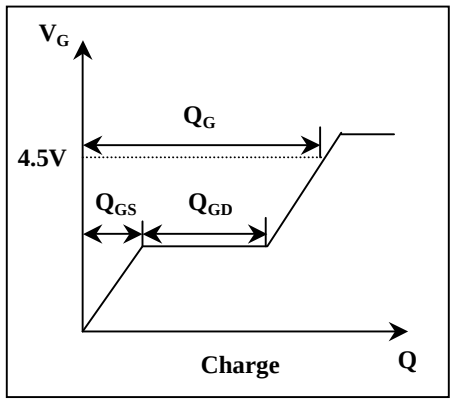
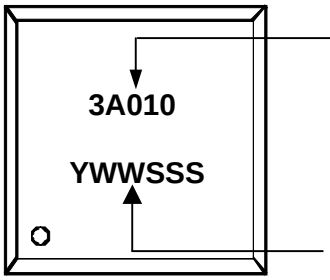



Fig 12. Gate Charge Waveform

## MARKING INFORMATION




Part Number

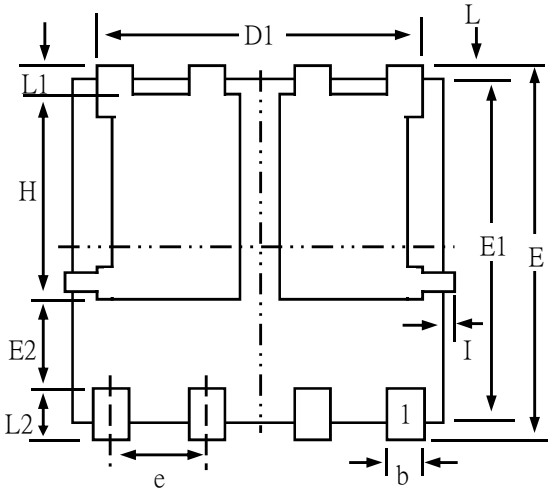
Date Code (YWWSSS)

Y：Last Digit Of The Year

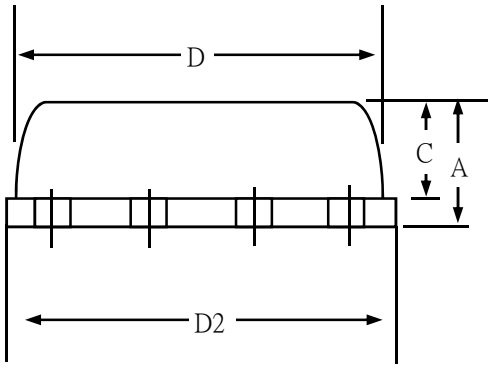
WW：Week

SSS：Sequence

# Package Outline : PMPAK 5x6 (Dual Pad)




BACKSIDE VIEW




| SYMBOLS | Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.80 | 1.00 | 1.20 |
| b | 0.34 | 0.42 | 0.50 |
| C | 0.54 | 0.76 | 0.97 |
| D | 4.80 | 4.95 | 5.10 |
| D1 | 4.11 | 4.21 | 4.31 |
| E | 5.90 | 6.05 | 6.20 |
| E1 | 5.60 | 5.75 | 5.90 |
| E2 | 1.60 (ref.) | | |
| e | 1.27 (ref.) | | |
| L | 0.05 | 0.15 | 0.25 |
| L1 | 0.60 (ref.) | | |
| L2 | 0.60 (ref.) | | |
| H | 3.60 (ref.) | | |
| I | 0.15 (ref.) | | |
| D2 | 4.80 | 5.15 | 5.50 |

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Mold Protrusions.

Draw No. M2-1MT8-G-v02

**PMPAK5X6(Dual Pad,左右) FOOTPRINT：**