



- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free

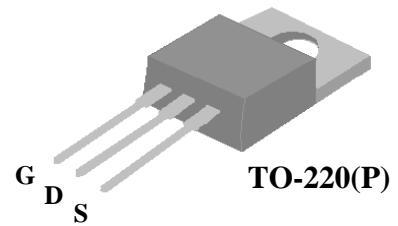


BV _{DSS}	30V
R _{DS(ON)}	2.1mΩ

Description

AP3N2R1 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.



Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	+20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Silicon Limited)	183	A
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴	130	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	129	A
I _{DM}	Pulsed Drain Current ¹	400	A
P _D @T _C =25°C	Total Power Dissipation	125	W
P _D @T _A =25°C	Total Power Dissipation	2.4	W
E _{AS}	Single Pulse Avalanche Energy ³	45	mJ
T _{STG}	Storage Temperature Range	-55 to 175	°C
T _J	Operating Junction Temperature Range	-55 to 175	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	1.2	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient	62	°C/W



AP3N2R1P

Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =60A	-	-	2.1	mΩ
		V _{GS} =4.5V, I _D =30A	-	-	3.3	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	3	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =60A	-	200	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =30A	-	71	113.6	nC
Q _{gs}	Gate-Source Charge	V _{DS} =24V	-	16	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	36	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	12	-	ns
t _r	Rise Time	I _D =40A	-	63	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	73	-	ns
t _f	Fall Time	V _{GS} =10V	-	110	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	6250	10000	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	1120	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	540	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.1	2.2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =60A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =40A, V _{GS} =0V,	-	28	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	17	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Starting T_j=25°C , V_{DD}=30V , L=0.1mH , R_G=25Ω
- 4.Package limitation current is 130A .

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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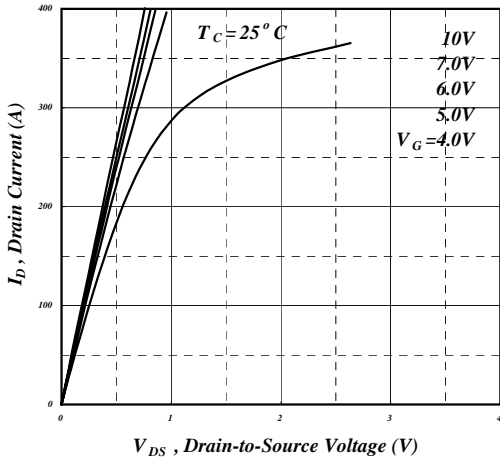


Fig 1. Typical Output Characteristics

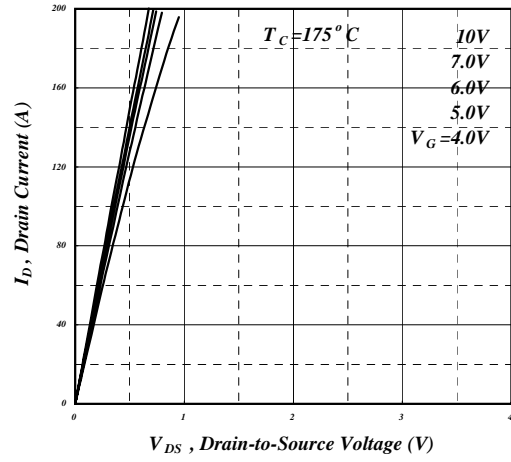


Fig 2. Typical Output Characteristics

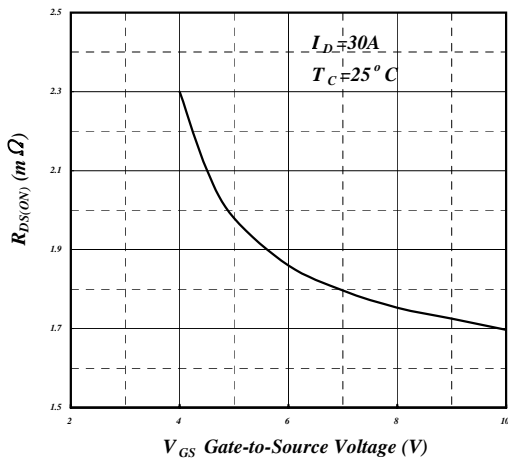


Fig 3. On-Resistance v.s. Gate Voltage

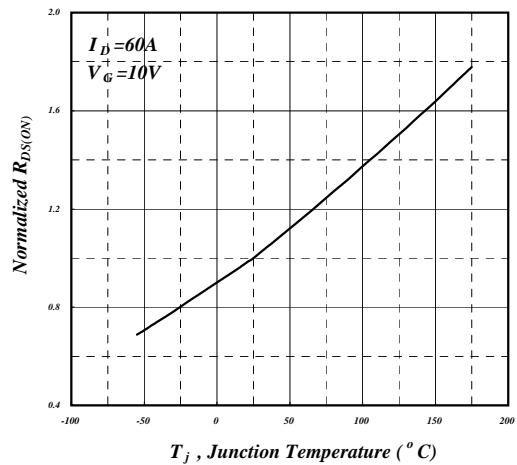


Fig 4. Normalized On-Resistance v.s. Junction Temperature

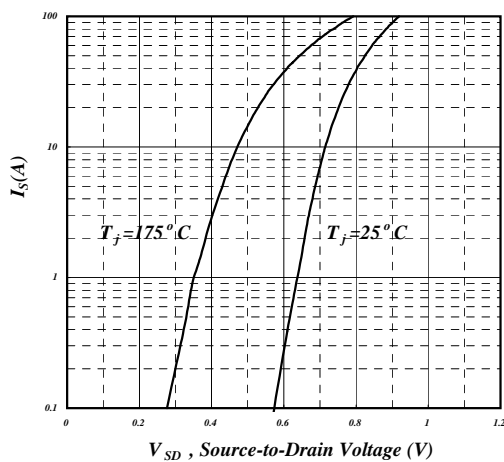


Fig 5. Forward Characteristic of Reverse Diode

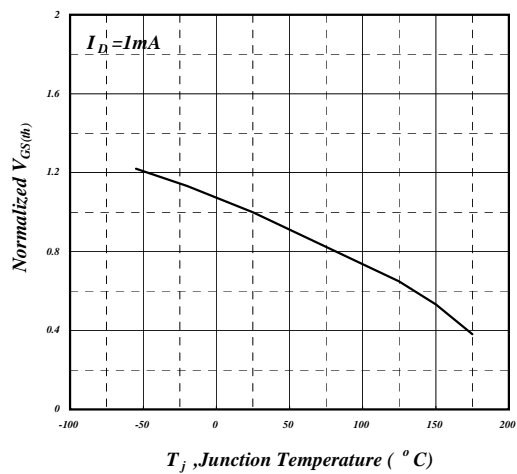


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

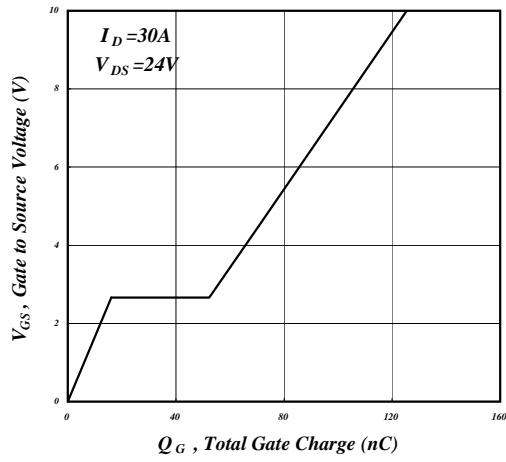


Fig 7. Gate Charge Characteristics

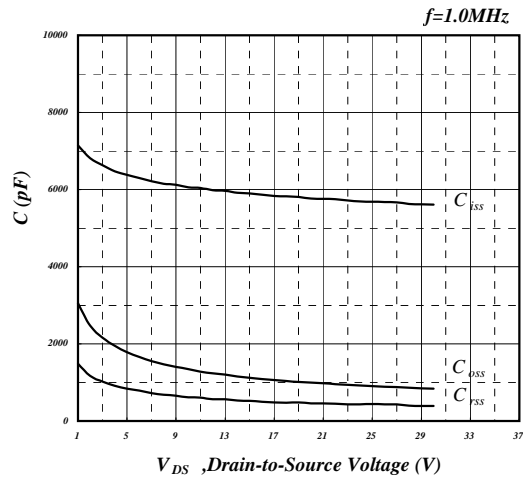


Fig 8. Typical Capacitance Characteristics

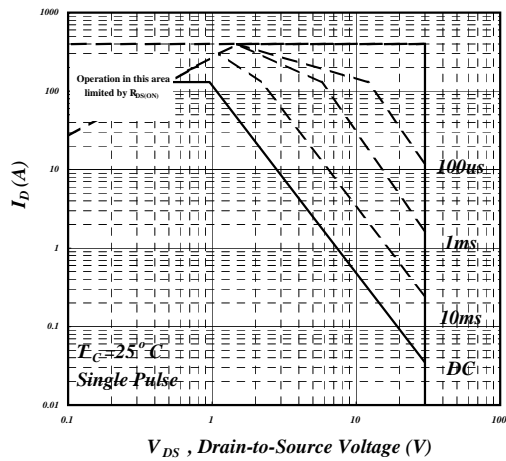


Fig 9. Maximum Safe Operating Area

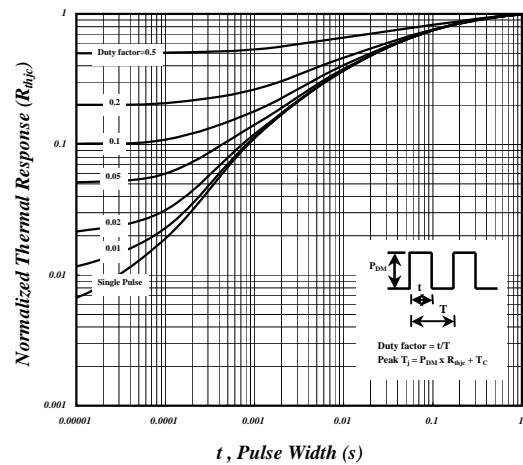


Fig 10. Effective Transient Thermal Impedance

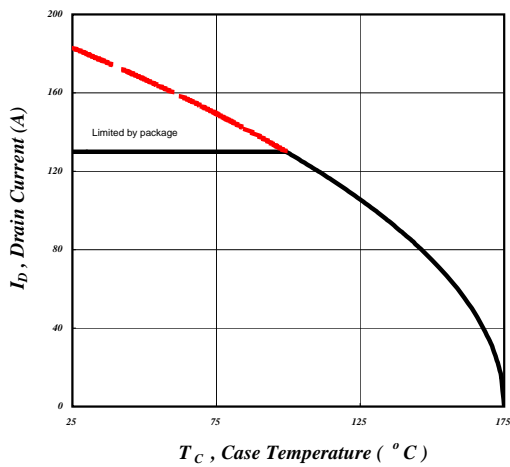


Fig 11. Drain Current v.s. Case Temperature

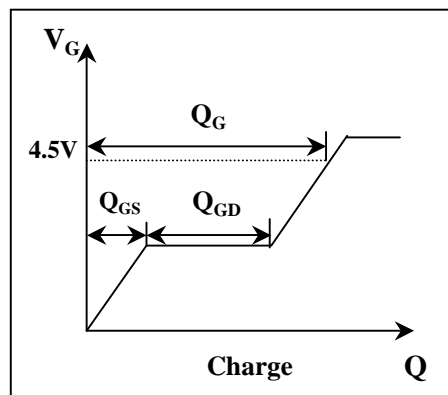


Fig 12. Gate Charge Circuit

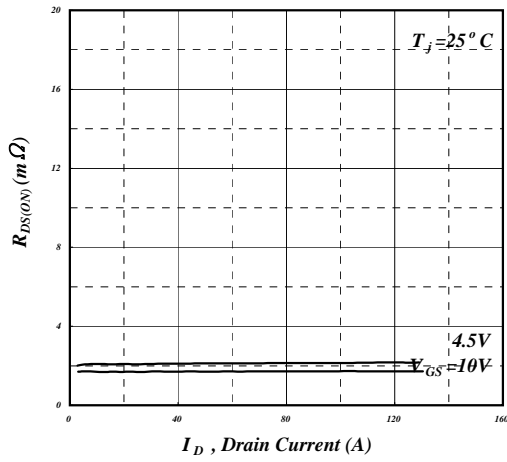


Fig 13. Typ. Drain-Source on State Resistance

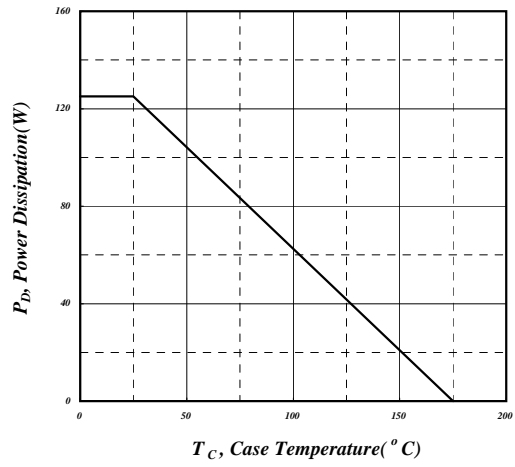


Fig 14. Total Power Dissipation

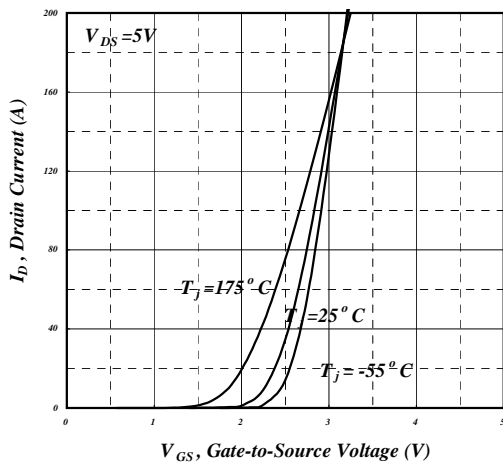
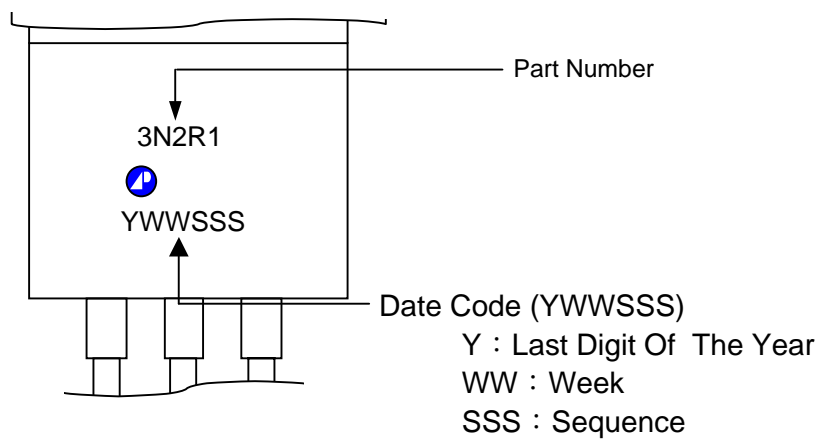


Fig 15. Transfer Characteristics



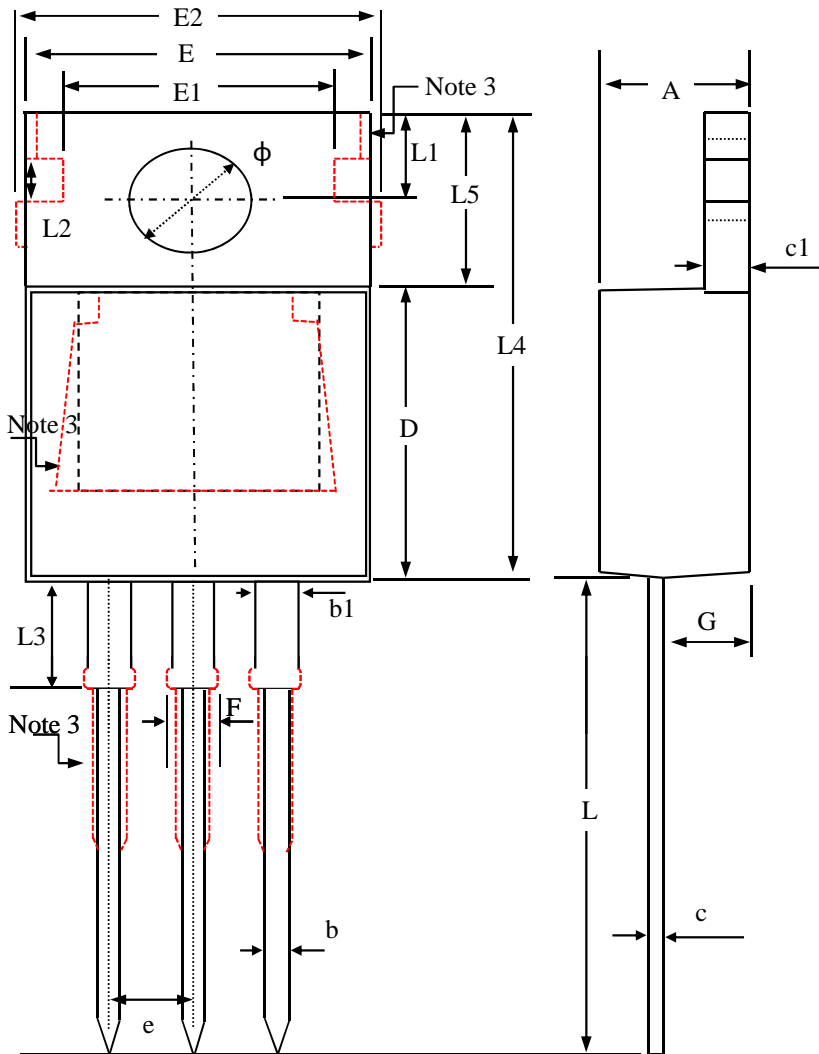
AP3N2R1P

MARKING INFORMATION





Package Outline : TO-220



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.20	4.50	4.80
b	0.60	0.80	1.00
b1	1.10	1.38	1.80
c	0.30	0.48	0.65
c1	1.10	1.30	1.50
E	9.70	10.00	10.40
E1	7.40	8.30	9.20
e	2.54 (ref.)		
L	12.70	13.60	14.50
L1	2.50	2.75	3.00
L2	1.00	1.40	1.80
L3	2.60	3.35	4.10
L4	14.30	15.15	16.00
L5	6.00	6.40	6.80
φ	3.40	3.70	4.00
D	8.30	8.85	9.40
F	1.20	1.41	1.85
G	2.20	2.60	3.00
E2	—	—	11.50

Note:

1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.



TO-220 FOOTPRINT :

