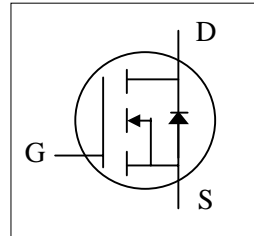
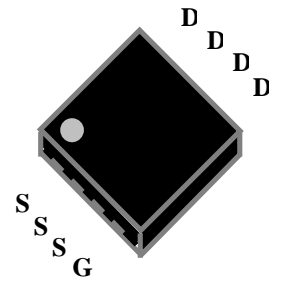




- ▼ Simple Drive Requirement
- ▼ Small Size & Low  $R_{DS(ON)}$
- ▼ RoHS Compliant & Halogen-Free



$BV_{DSS}$	30V
$R_{DS(ON)}$	9.5m $\Omega$



**PMPAK<sup>®</sup> 3 x 3**

### Description

AP3N9R5 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK<sup>®</sup> 3 x 3 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

### Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}$	37.8	A
$I_D @ T_A=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	15	A
$I_D @ T_A=70^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	12	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	100	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	3.57	W
$E_{AS}$	Single Pulse Avalanche Energy <sup>4</sup>	16.2	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	5.5	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	35	$^\circ\text{C}/\text{W}$



# AP3N9R5YT

## Electrical Characteristics @T<sub>j</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =9.5A	-	-	9.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =9A	-	-	14.5	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =9.5A	-	35	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V	-	-	10	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =9.5A	-	24	38.4	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =15V	-	4	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =10V	-	6	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =15V	-	9	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =9.5A	-	30	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3Ω	-	23	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	5	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	1000	1600	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =15V	-	155	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	120	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	1.6	3.2	Ω

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =3A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =9.5A, V <sub>GS</sub> =0V,	-	11	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	4	-	nC

### Notes:

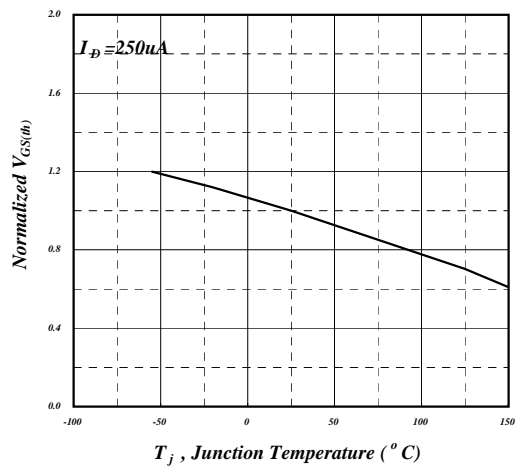
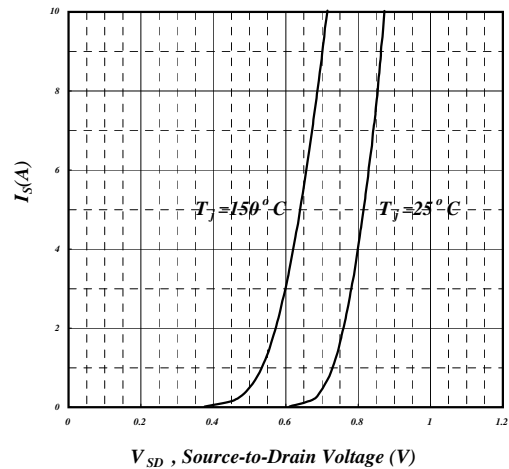
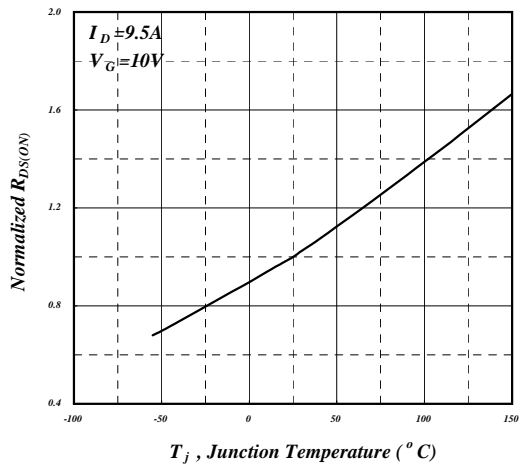
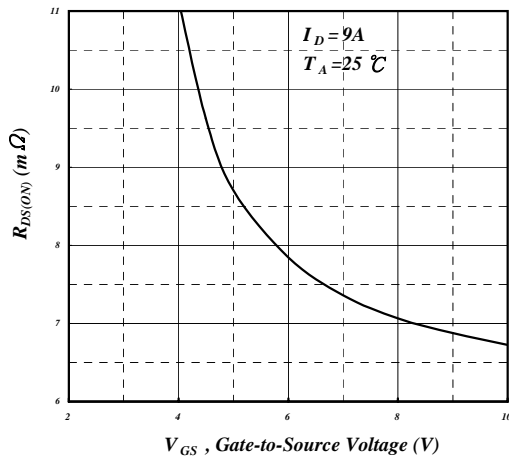
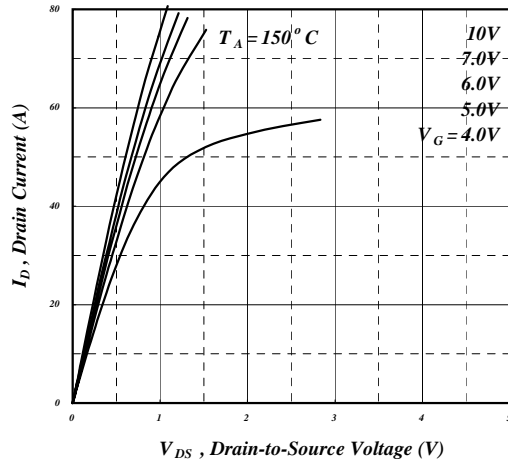
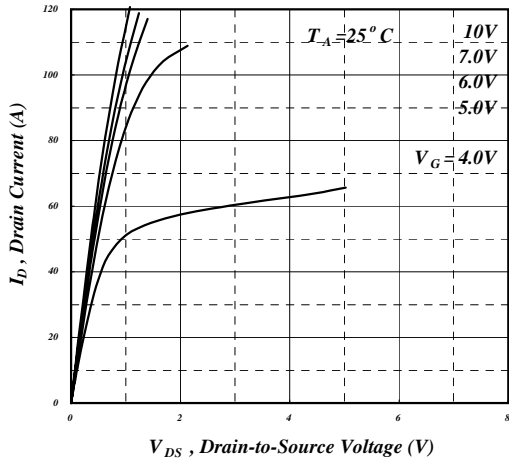
1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> 2oz copper pad of FR4 board, t ≤10sec; 160°C/W when mounted on min. copper pad.
4. Starting T<sub>j</sub>=25°C, V<sub>DD</sub>=30V, L=0.1mH, R<sub>G</sub>=25Ω, V<sub>GS</sub>=10V

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



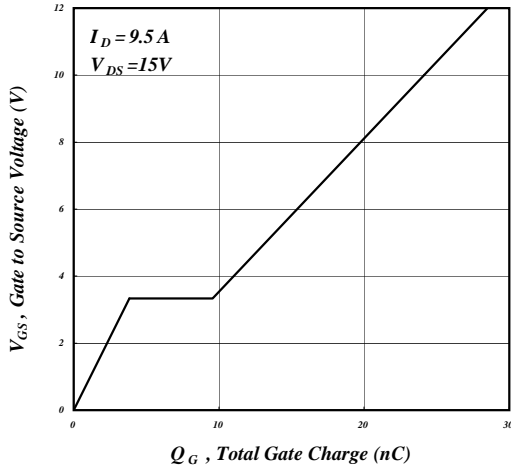


Fig 7. Gate Charge Characteristics

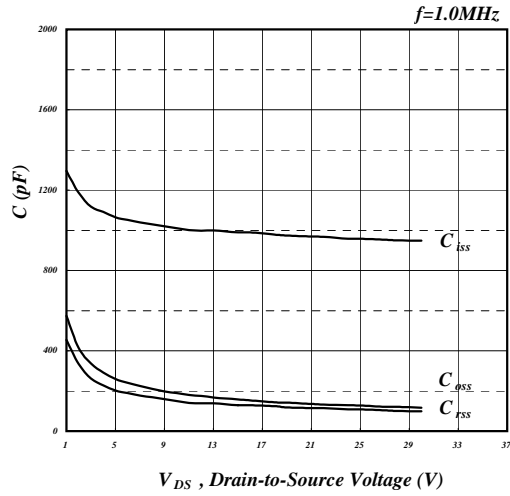


Fig 8. Typical Capacitance Characteristics

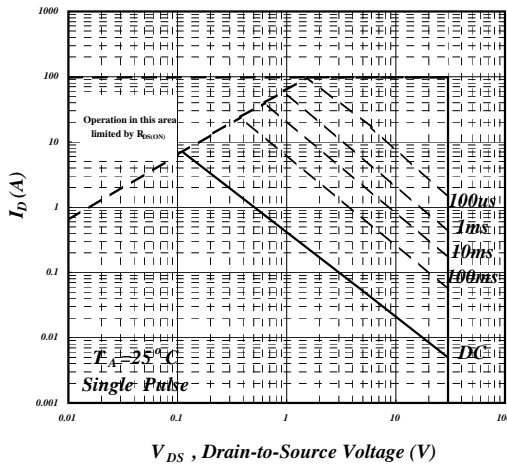


Fig 9. Maximum Safe Operating Area

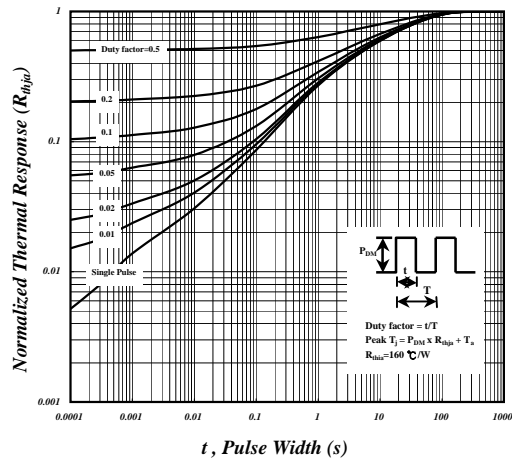


Fig 10. Effective Transient Thermal Impedance

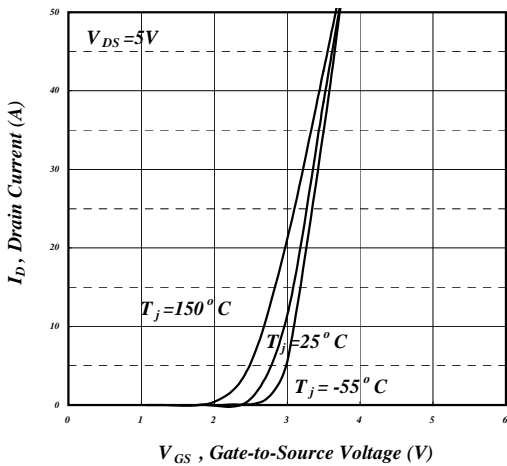


Fig 11. Transfer Characteristics

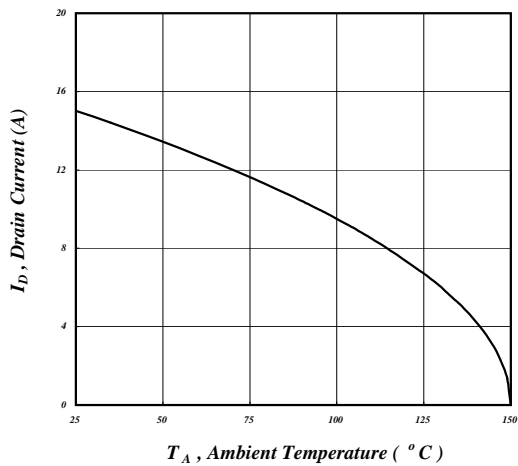


Fig 12. Drain Current v.s. Ambient Temperature

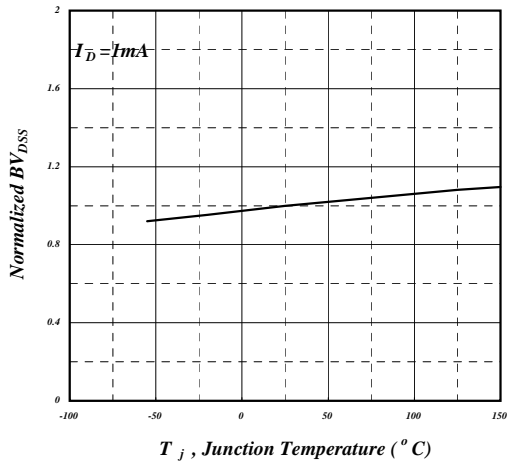


Fig 13. Normalized  $BV_{DSS}$  v.s. Junction

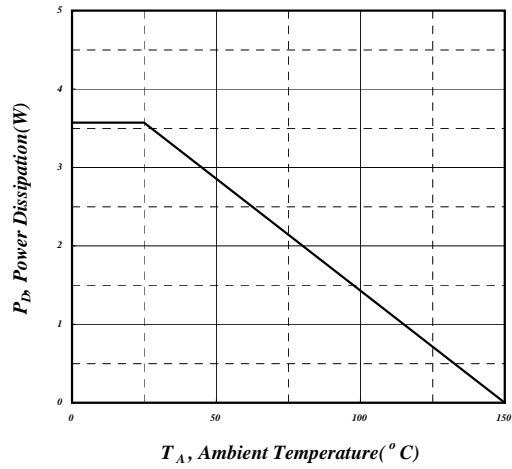


Fig 14. Total Power Dissipation

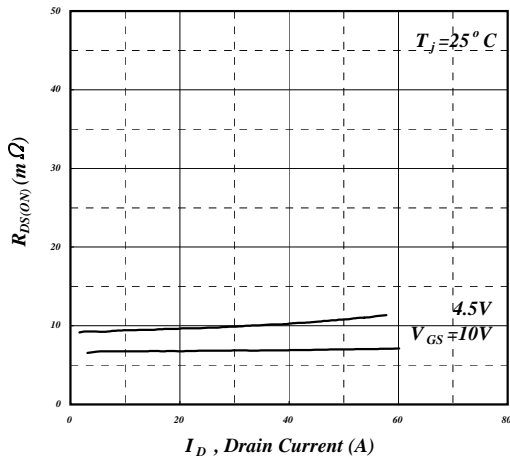


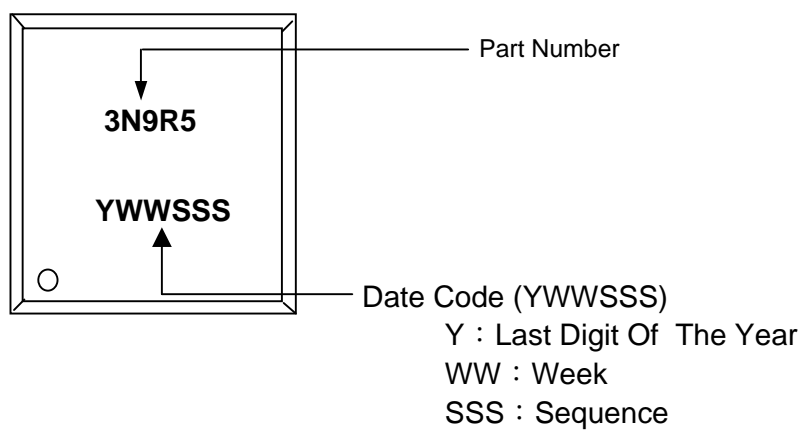
Fig 15. Typ. Drain-Source on State Resistance



**AP3N9R5YT**

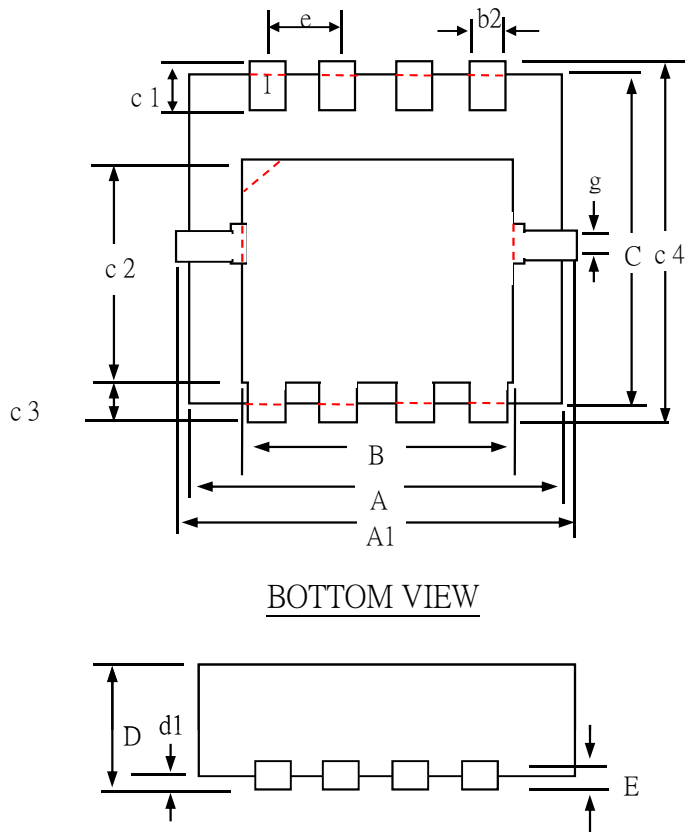
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**MARKING INFORMATION**





## Package Outline : PMPAK 3x3



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	2.90	3.10	3.40
B	2.20	2.45	2.80
e	0.60	0.65	0.70
b2	0.20	0.30	0.40
C	2.90	3.10	3.40
c1	0.10	0.30	0.50
c2	1.20	1.70	2.20
c3	0.10	0.38	0.65
D	0.65	0.80	1.05
d1	0.00	0.10	0.20
E	0.10	0.18	0.25
A1	2.900	3.30	3.600
c4	2.900	3.30	3.600
g	0.20 (ref)		

1. All Dimension Are In Millimeters.
2. Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.



PMPAK3X3 FOOTPRINT :

