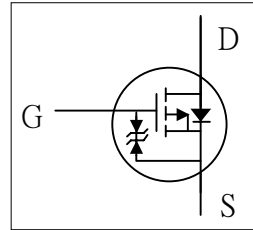




- ▼ 100% R<sub>g</sub> & UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free

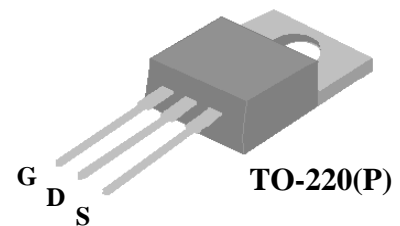


BV <sub>DSS</sub>	-30V
R <sub>DS(ON)</sub>	7mΩ
I <sub>D</sub>	-75A
HBM ESD	2KV

## Description

AP3P7R0E series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.



## Absolute Maximum Ratings @T<sub>j</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	-30	V
V <sub>GS</sub>	Gate-Source Voltage	+20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Drain Current, V <sub>GS</sub> @ 10V	-75	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Drain Current, V <sub>GS</sub> @ 10V	-47.8	A
I <sub>DM</sub>	Pulsed Drain Current <sup>1</sup>	-300	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	59.5	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation	2	W
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>3</sup>	135	mJ
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

## Thermal Data

Symbol	Parameter	Value	Units
R <sub>thj-c</sub>	Maximum Thermal Resistance, Junction-case	2.1	°C/W
R <sub>thj-a</sub>	Maximum Thermal Resistance, Junction-ambient	62	°C/W



# AP3P7R0EP

## Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-30A$	-	-	7	m $\Omega$
		$V_{GS}=-4.5V, I_D=-20A$	-	-	15	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-30A$	-	55	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V$	-	-	-10	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 30$	$\mu A$
$Q_g$	Total Gate Charge	$I_D=-20A$	-	36	57.6	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=-24V$	-	10	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	15	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=-15V$	-	42	-	ns
$t_r$	Rise Time	$I_D=-30A$	-	140	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	440	-	ns
$t_f$	Fall Time	$V_{GS}=-10V$	-	300	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	4300	6880	pF
$C_{oss}$	Output Capacitance	$V_{DS}=-15V$	-	590	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	330	-	pF

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=-30A, V_{GS}=0V$	-	-	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_S=-30A, V_{GS}=0V,$	-	18	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	6	-	nC

### Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Starting  $T_j=25^{\circ}\text{C}$ ,  $V_{DD}=-30V$ ,  $L=0.3\text{mH}$ ,  $R_G=25\Omega$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

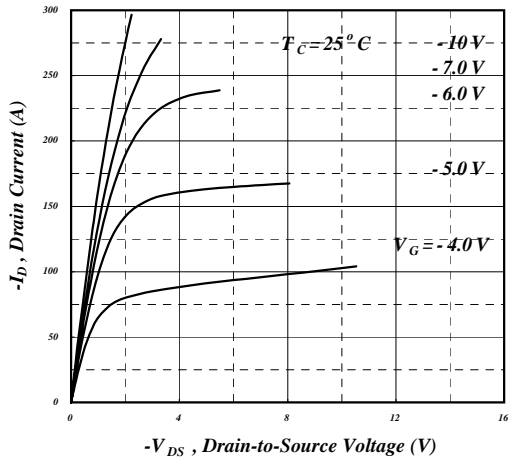


Fig 1. Typical Output Characteristics

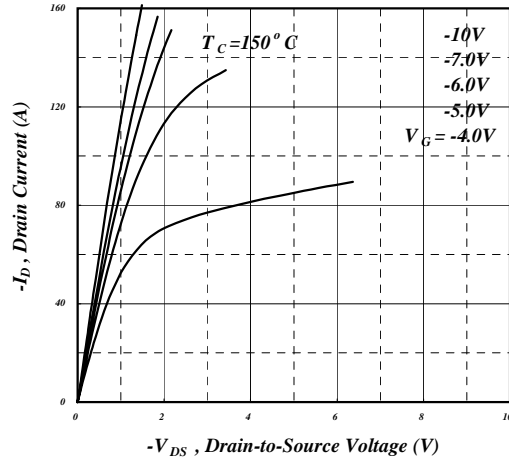


Fig 2. Typical Output Characteristics

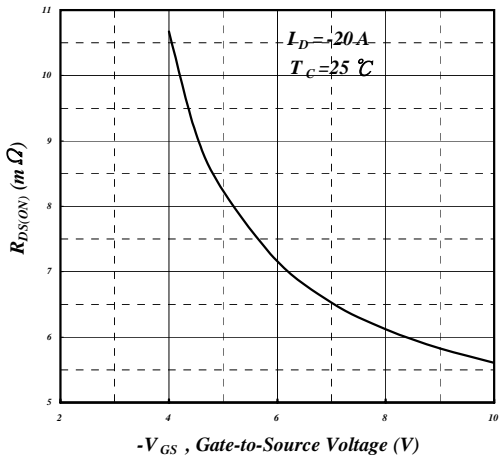


Fig 3. On-Resistance v.s. Gate Voltage

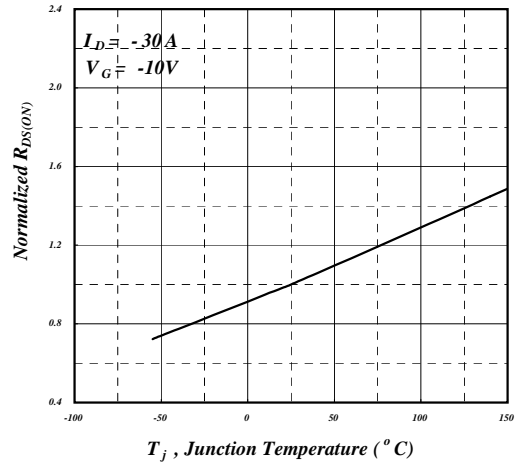


Fig 4. Normalized On-Resistance v.s. Junction Temperature

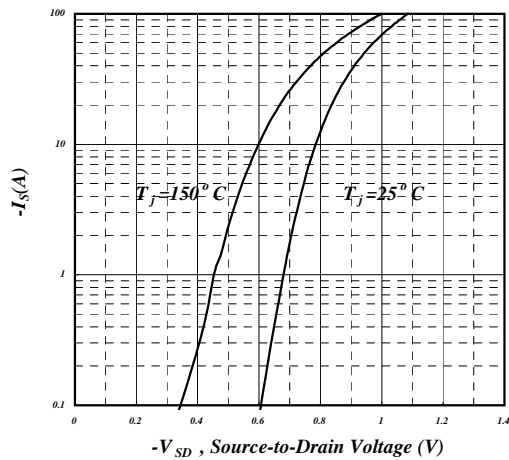


Fig 5. Forward Characteristic of Reverse Diode

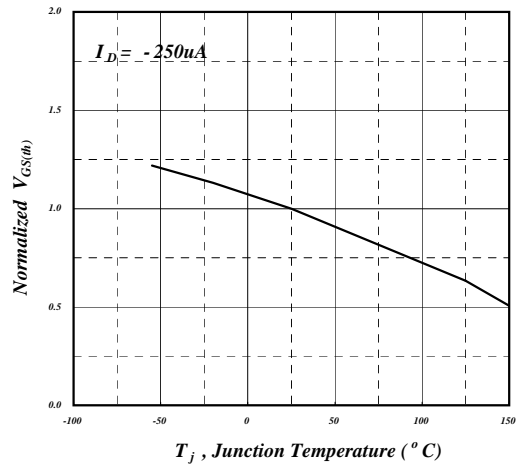


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

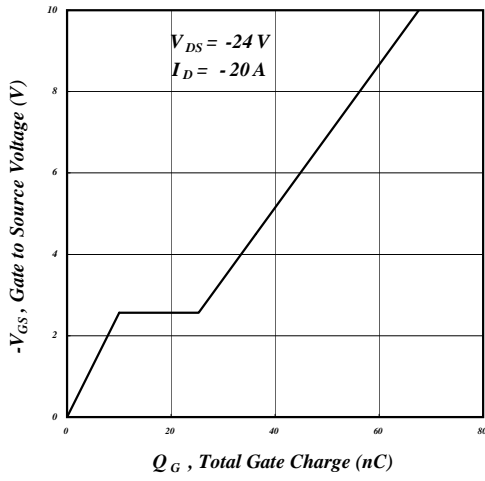


Fig 7. Gate Charge Characteristics

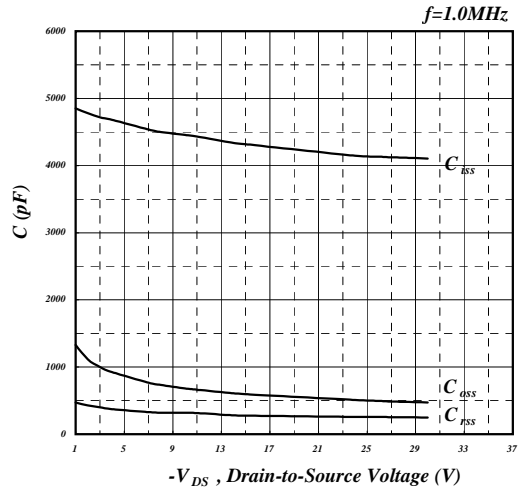


Fig 8. Typical Capacitance Characteristics

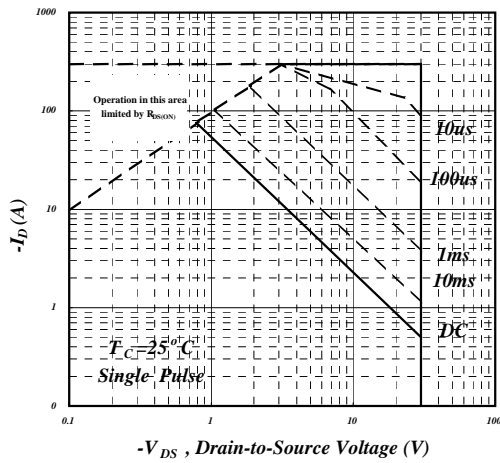


Fig 9. Maximum Safe Operating Area

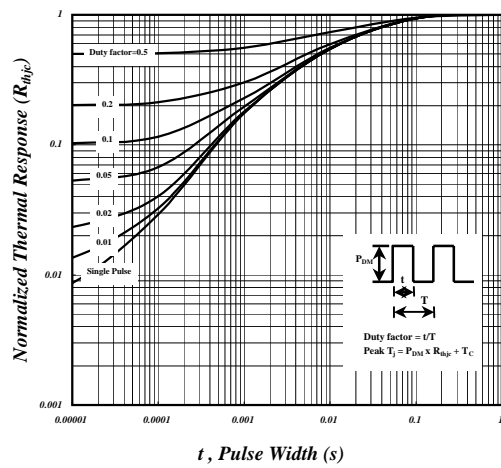


Fig 10. Effective Transient Thermal Impedance

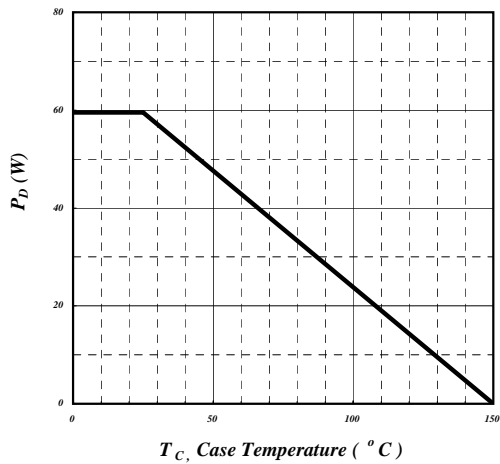


Fig 11. Typical Power Dissipation

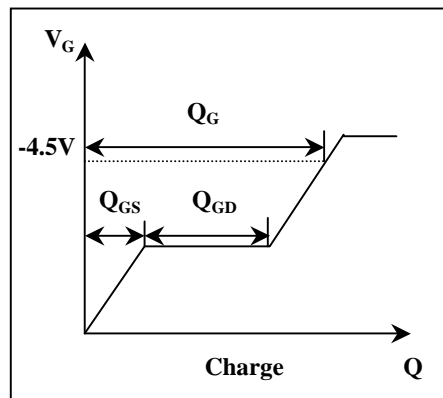


Fig 12. Gate Charge Waveform

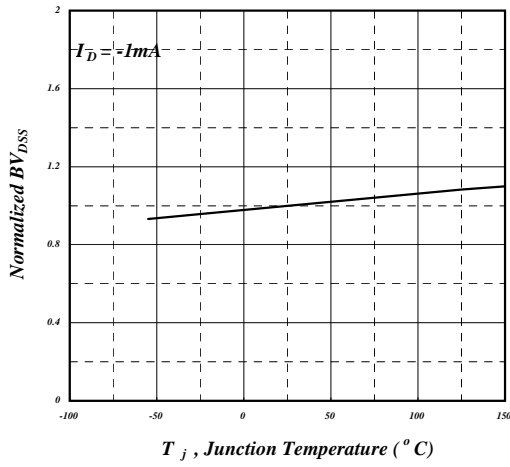


Fig 13. Normalized  $BV_{DSS}$  v.s. Junction Temperature

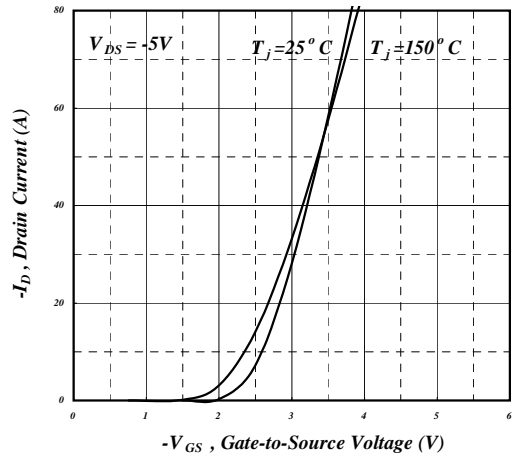


Fig 14. Transfer Characteristics

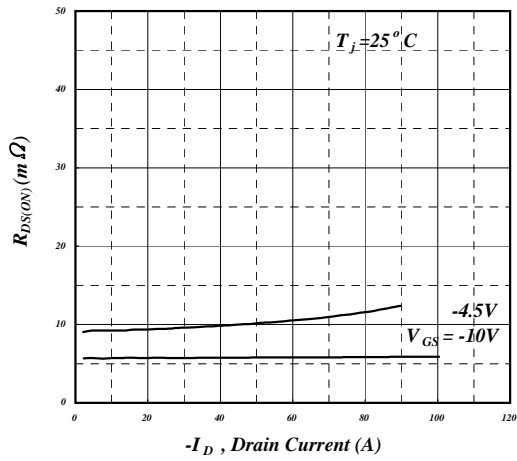


Fig 15. Typ. Drain-Source on State Resistance

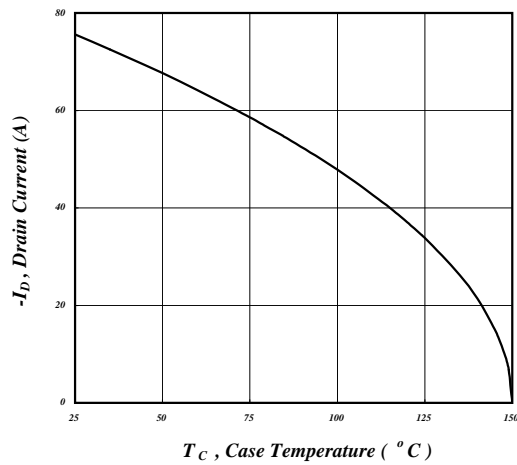
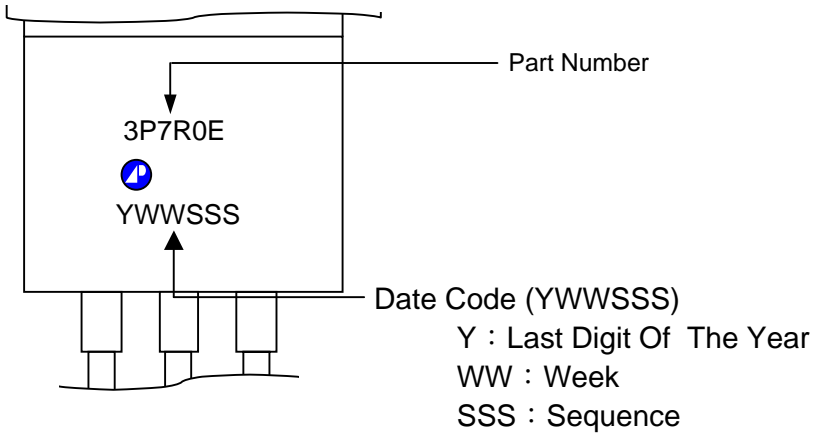


Fig 16. Drain Current v.s. Case Temperature



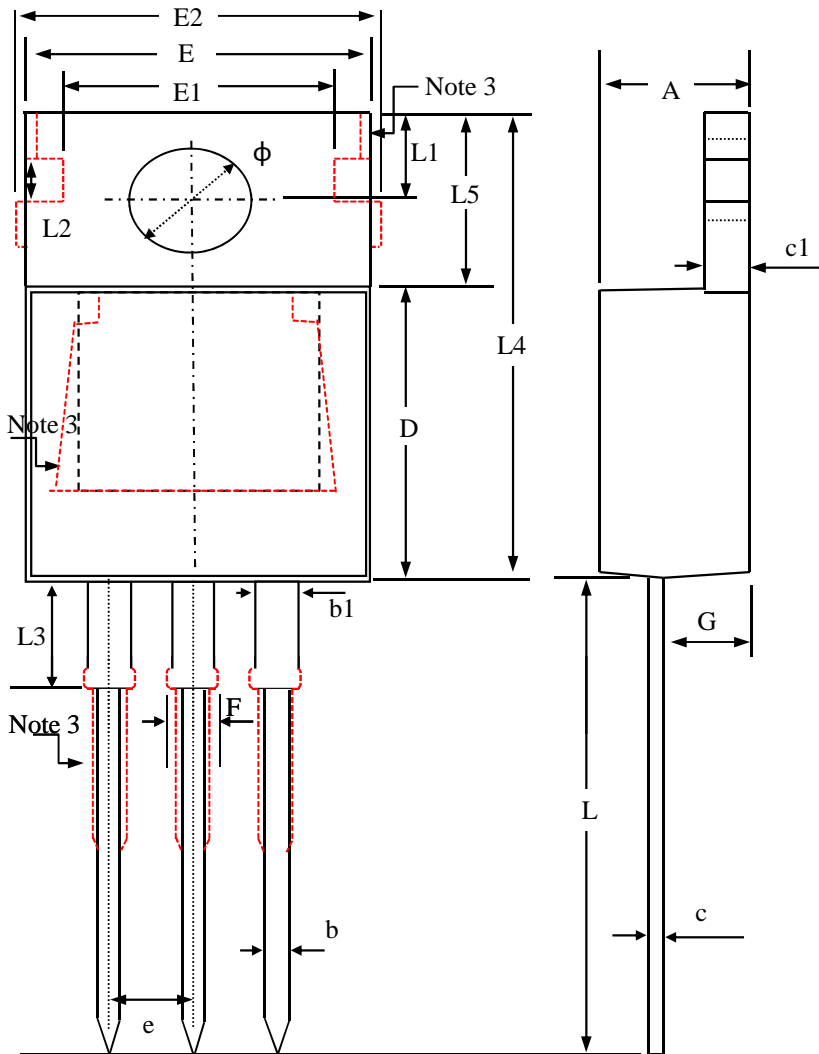
# AP3P7R0EP

## MARKING INFORMATION





## Package Outline : TO-220



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.20	4.50	4.80
b	0.60	0.80	1.00
b1	1.10	1.38	1.80
c	0.30	0.48	0.65
c1	1.10	1.30	1.50
E	9.70	10.00	10.40
E1	7.40	8.30	9.20
e	2.54 (ref.)		
L	12.70	13.60	14.50
L1	2.50	2.75	3.00
L2	1.00	1.40	1.80
L3	2.60	3.35	4.10
L4	14.30	15.15	16.00
L5	6.00	6.40	6.80
$\phi$	3.40	3.70	4.00
D	8.30	8.85	9.40
F	1.20	1.41	1.85
G	2.20	2.60	3.00
E2	—	—	11.50

Note:

1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.



**TO-220 FOOTPRINT :**

