



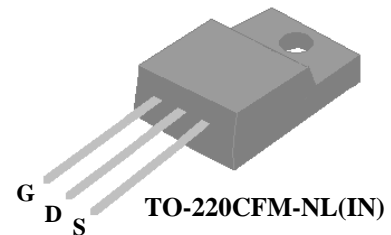
- ▼ 100% UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



$BV_{DSS}$	500V
$R_{DS(ON)}$	0.27 $\Omega$
$I_D^3$	18A

## Description

AP50AN270 series are from the innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.



The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.

## Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	500	V
$V_{GS}$	Gate-Source Voltage	$\pm 30$	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	18	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	72	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	41.6	W
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	1.92	W
$E_{AS}$	Single Pulse Avalanche Energy <sup>4</sup>	37	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ\text{C}/\text{W}$



# AP50AN270IN

## Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	500	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =9A	-	-	0.27	Ω
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	-	4	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =20V, I <sub>D</sub> =9A	-	25	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V	-	-	100	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	-	-	±1	uA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =18A	-	72	115	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =400V	-	14	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =10V	-	27	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =250V	-	22	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =18A	-	49	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =10Ω	-	110	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	60	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	2900	4640	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =100V	-	150	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	11	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	2.5	5	Ω

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =9A, V <sub>GS</sub> =0V	-	-	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =18A, V <sub>GS</sub> =0V	-	380	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	4.3	-	uC

### Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse test
- 3.Ensure that the junction temperature does not exceed T<sub>Jmax</sub>.
- 4.Starting T<sub>j</sub>=25°C , V<sub>DD</sub>=90V , L=1mH , R<sub>G</sub>=25Ω , V<sub>GS</sub>=10V

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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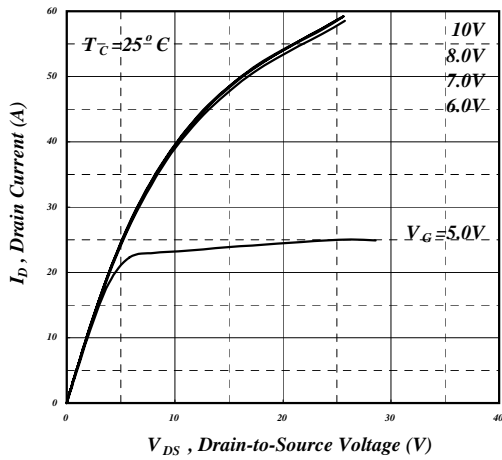


Fig 1. Typical Output Characteristics

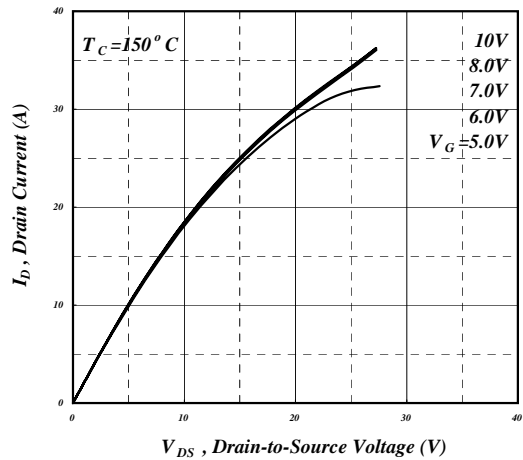


Fig 2. Typical Output Characteristics

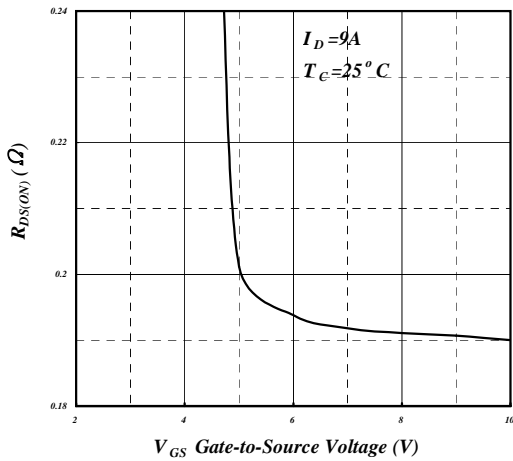


Fig 3. On-Resistance v.s. Gate Voltage

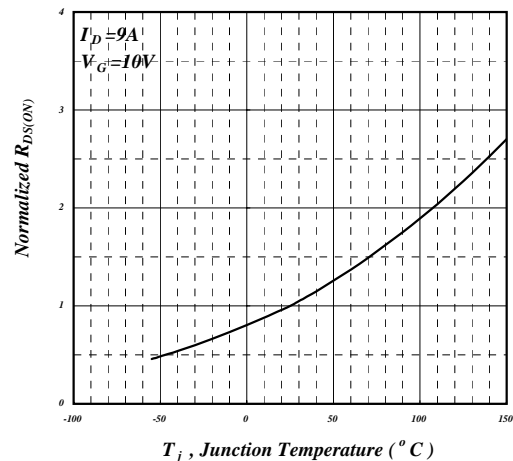


Fig 4. Normalized On-Resistance v.s. Junction Temperature

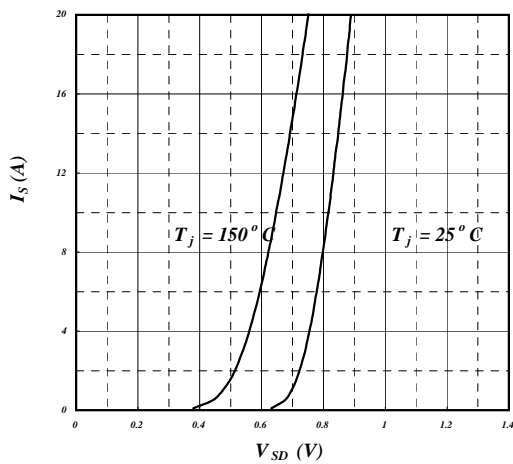


Fig 5. Forward Characteristic of Reverse Diode

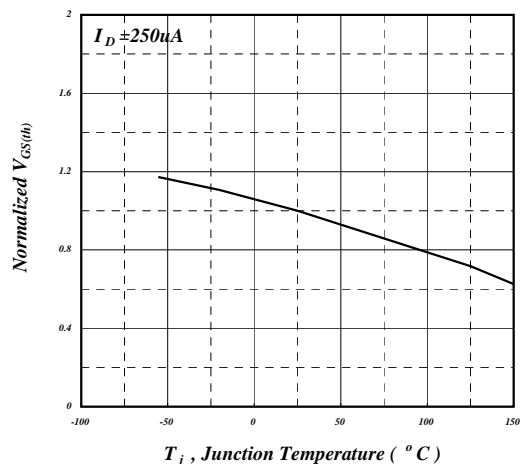


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

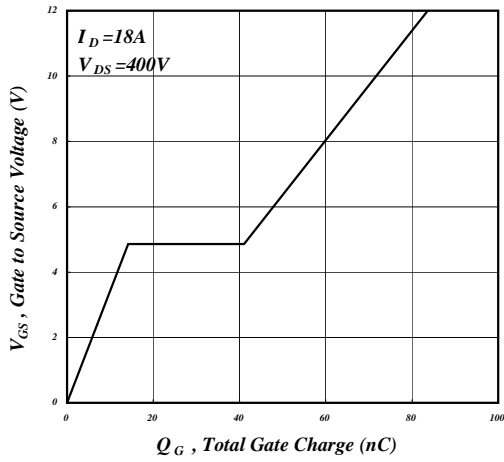


Fig 7. Gate Charge Characteristics

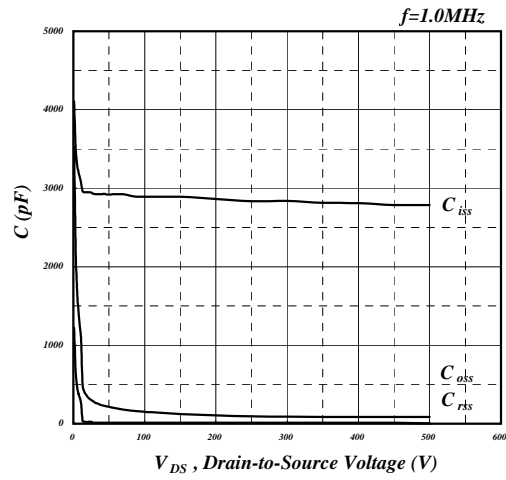


Fig 8. Typical Capacitance Characteristics

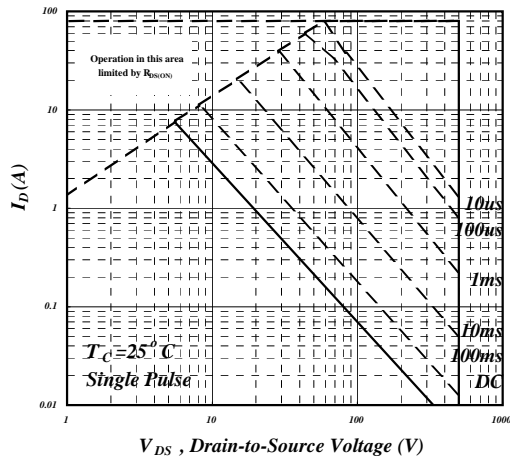


Fig 9. Maximum Safe Operating Area

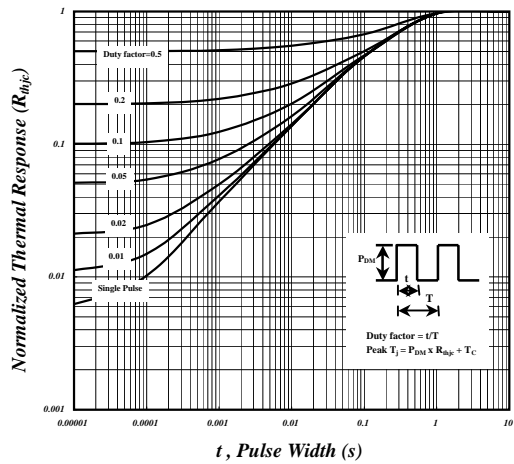


Fig 10. Effective Transient Thermal Impedance

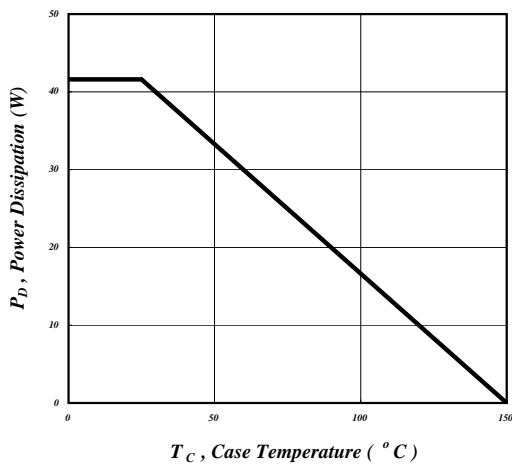


Fig 11. Total Power Dissipation

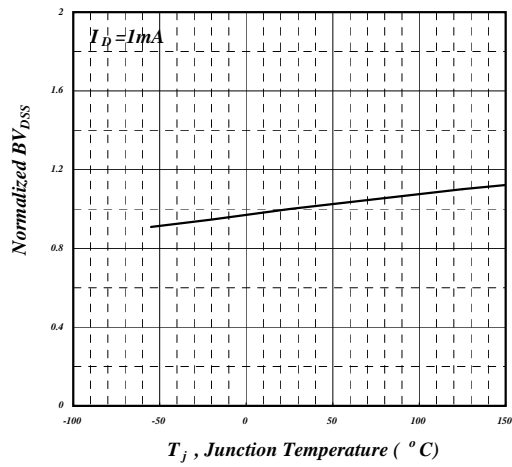
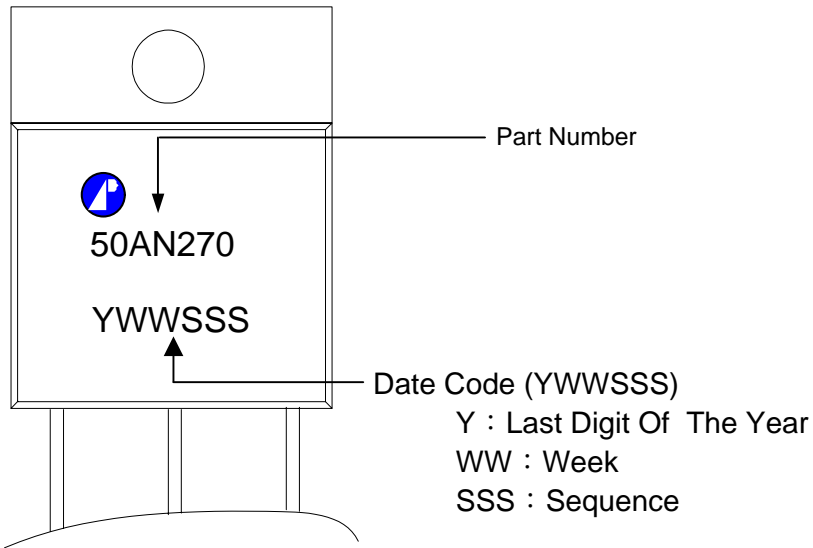


Fig 12. Normalized  $BV_{DSS}$  v.s. Junction Temperature



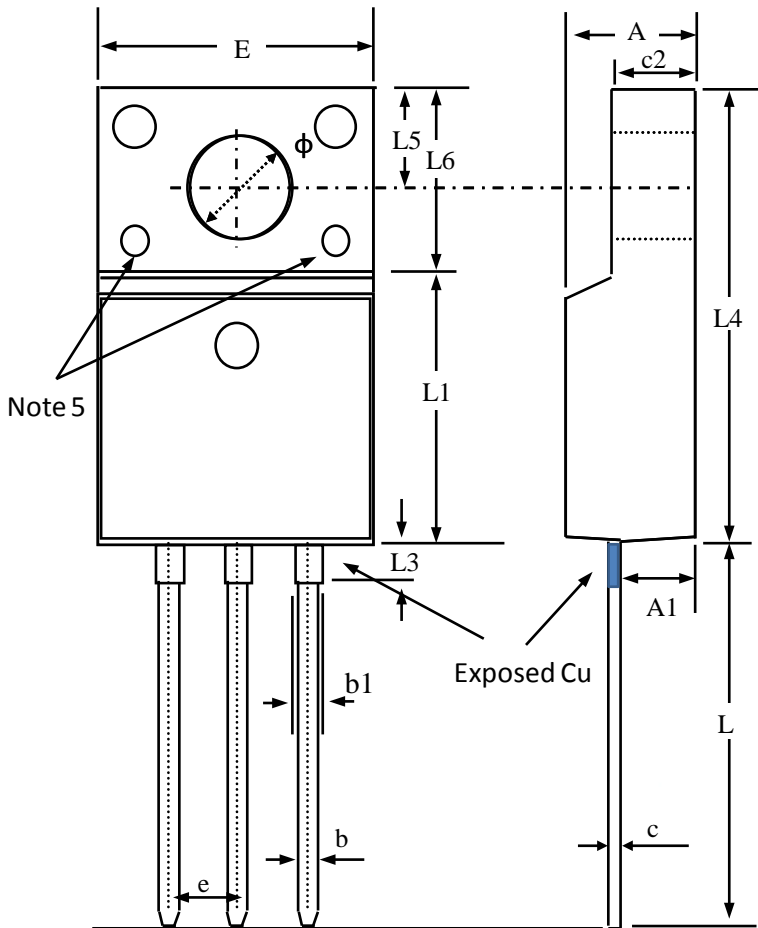
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**MARKING INFORMATION**





## Package Outline : TO-220CFM-NL



SYMBOLS	Millimeters		
	MIN	NOM	MAX
<b>A</b>	4.30	4.50	4.70
<b>A1</b>	2.50	2.60	2.70
<b>b</b>	0.60	0.70	0.80
<b>b1</b>	0.60	0.80	0.90
<b>c</b>	0.45	0.50	0.60
<b>c2</b>	2.50	2.70	2.90
<b>E</b>	9.70	10.00	10.30
<b>L</b>	13.40	13.60	13.80
<b>L1</b>		8.5 (ref.)	
<b>L3</b>	1.00	1.10	1.20
<b>L4</b>	14.70	15.00	15.30
<b>L5</b>	2.90	3.00	3.10
<b>L6</b>	6.30	6.50	6.70
$\phi$	3.00	3.20	3.40
<b>e</b>	2.60 (BSC)		

1. All Dimensions Are in Millimeters.
2. Package body sizes exclude mold flash and burrs  
mold flash should be less than 10 mil.
3. Stand off 1.10mm.
4. Ejector pin on package hole:  $\phi 1.5$  dep 0.1mm
5. Potting process option for these two holes



**TO-220CFM-NL FOOTPRINT :**

