



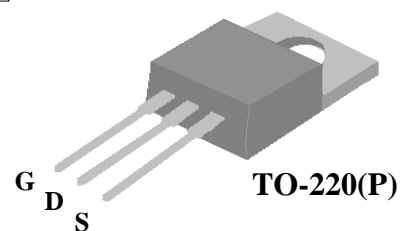
- ▼ 100% UIS Test
- ▼ Simple Drive Requirement
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	500V
$R_{DS(ON)}$	0.5Ω
I_D^3	13A

Description

AP50AN500 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.



The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.

Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	13	A
I_{DM}	Pulsed Drain Current ¹	52	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	125	W
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2	W
E_{AS}	Single Pulse Avalanche Energy ⁴	84.5	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$



AP50AN500P

Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	500	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=6.5A$	-	-	0.5	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance	$V_{DS}=20V, I_D=6.5A$	-	17.5	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=400V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	± 1	μA
Q_g	Total Gate Charge	$I_D=13A$	-	40	64	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=400V$	-	8	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	16	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=250V$	-	23	-	ns
t_r	Rise Time	$I_D=13A$	-	44	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=25\Omega$	-	110	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	55	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1540	2464	pF
C_{oss}	Output Capacitance	$V_{DS}=100V$	-	82	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	-	9	-	pF
R_g	Gate Resistance	$f=1.0MHz$	-	1.4	2.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=6.5A, V_{GS}=0V$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=13A, V_{GS}=0V$	-	360	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	3.3	-	μC

Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse test
- 3.Ensure that the junction temperature does not exceed T_{Jmax} .
- 4.Starting $T_j=25^\circ C$, $V_{DD}=90V$, $L=1mH$, $R_G=25\Omega$, $V_{GS}=10V$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

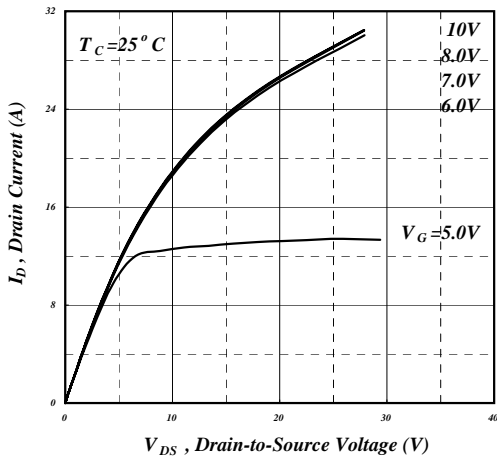


Fig 1. Typical Output Characteristics

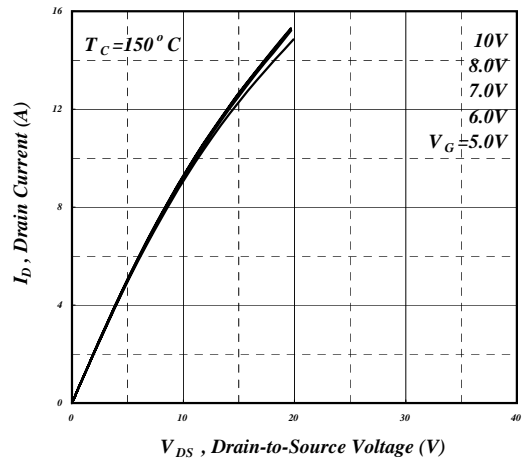


Fig 2. Typical Output Characteristics

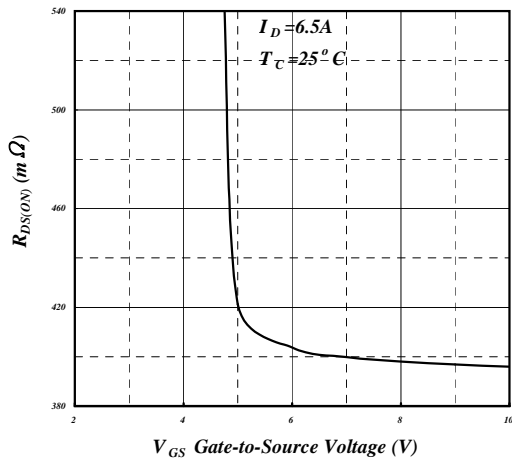


Fig 3. On-Resistance v.s. Gate Voltage

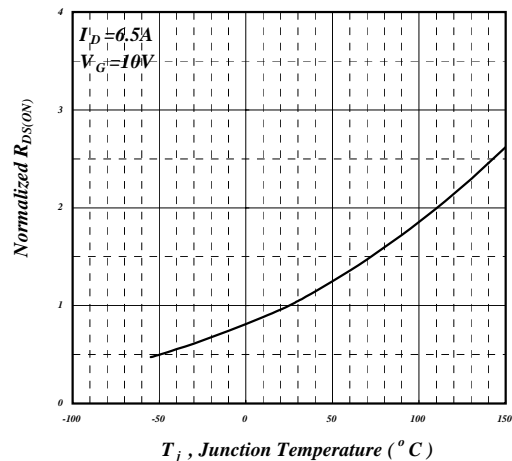


Fig 4. Normalized On-Resistance v.s. Junction Temperature

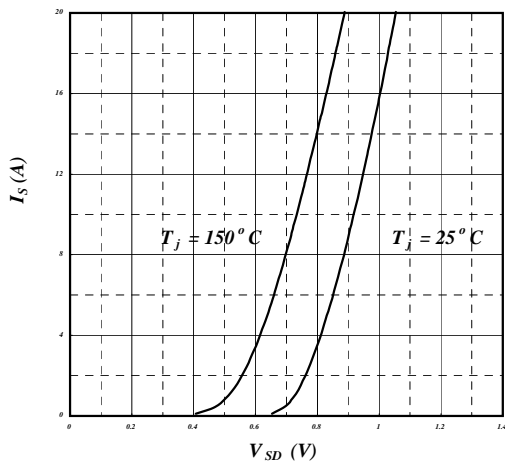


Fig 5. Forward Characteristic of Reverse Diode

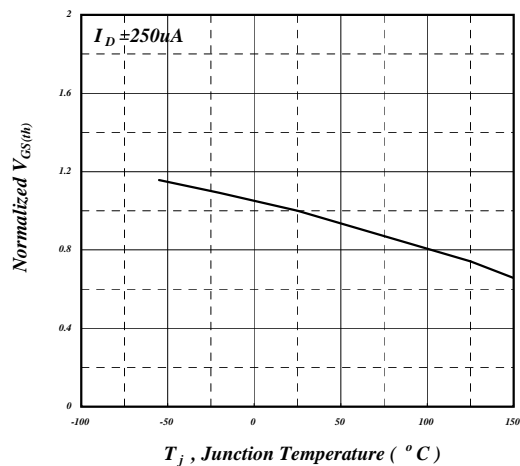


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

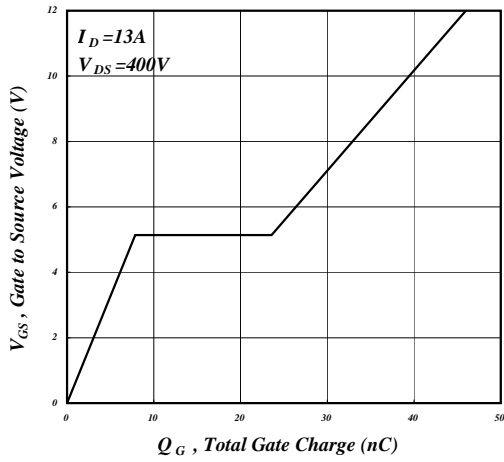


Fig 7. Gate Charge Characteristics

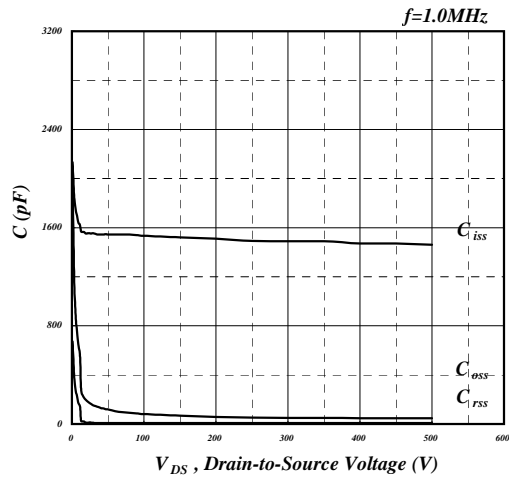


Fig 8. Typical Capacitance Characteristics

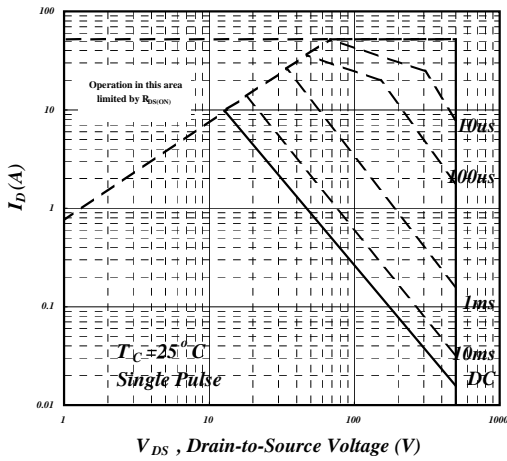


Fig 9. Maximum Safe Operating Area

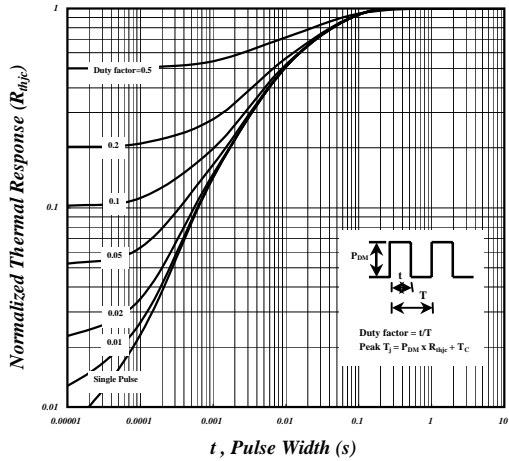


Fig10. Effective Transient Thermal Impedance

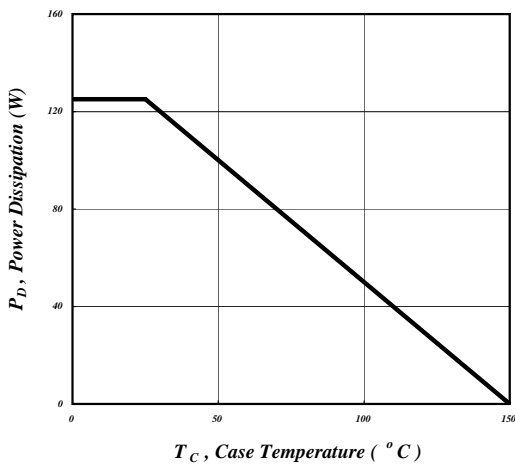


Fig 11. Total Power Dissipation

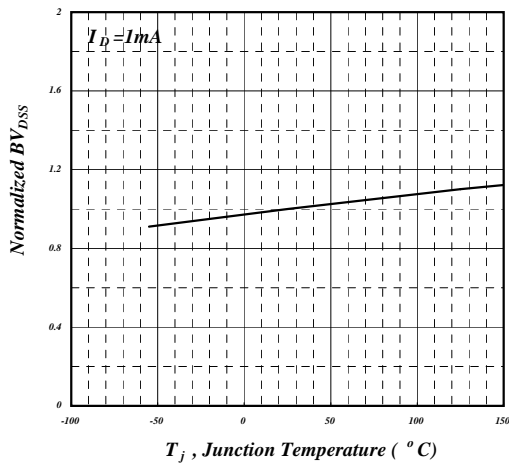
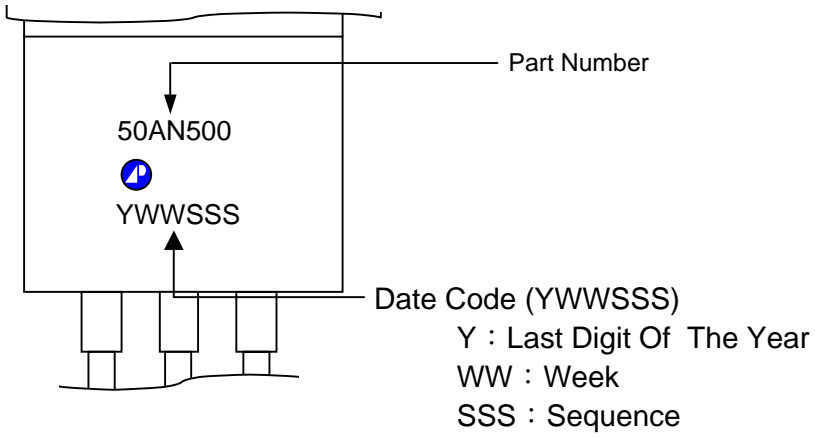


Fig 12. Normalized BV_{DSS} v.s. Junction Temperature

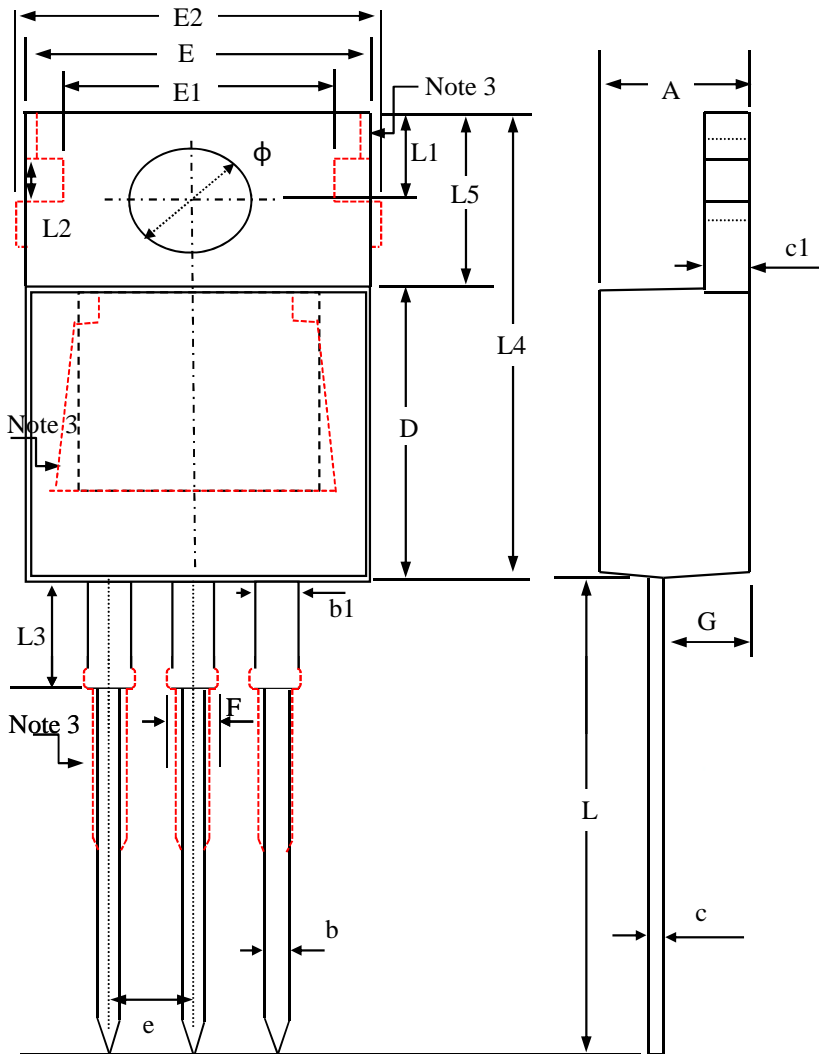


MARKING INFORMATION





Package Outline : TO-220



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.20	4.50	4.80
b	0.60	0.80	1.00
b1	1.10	1.38	1.80
c	0.30	0.48	0.65
c1	1.10	1.30	1.50
E	9.70	10.00	10.40
E1	7.40	8.30	9.20
e	2.54 (ref.)		
L	12.70	13.60	14.50
L1	2.50	2.75	3.00
L2	1.00	1.40	1.80
L3	2.60	3.35	4.10
L4	14.30	15.15	16.00
L5	6.00	6.40	6.80
ϕ	3.40	3.70	4.00
D	8.30	8.85	9.40
F	1.20	1.41	1.85
G	2.20	2.60	3.00
E2	—	—	11.50

Note:

1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.



TO-220 FOOTPRINT :

