

AP60SL650AFH

Halogen-Free Product

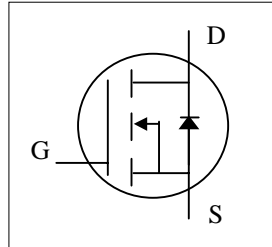


**Advanced Power
Electronics Corp.**

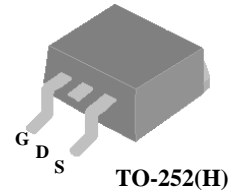
N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% R_g & UIS Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV _{DSS}	600V
R _{DS(ON)}	0.65 Ω
I _D ³	5.8A



Description

AP60SL650AF series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	600	V
V _{GS}	Gate-Source Voltage	±20	V
V _{GS}	Gate-Source Voltage, AC (f > 1Hz)	±30	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ³	5.8	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V ³	3.7	A
I _{DM}	Pulsed Drain Current ¹	18	A
dv/dt	MOSFET dv/dt Ruggedness (V _{DS} = 0 ...400V)	40	V/ns
P _D @T _C =25°C	Total Power Dissipation	56.8	W
P _D @T _A =25°C	Total Power Dissipation	2	W
E _{AS}	Single Pulse Avalanche Energy ⁴	36.7	mJ
dv/dt	Peak Diode Recovery dv/dt ⁵	15	V/ns
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	2.2	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁶	62.5	°C/W



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Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =1mA	600	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =2A	-	-	0.65	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	5	V
g _{fs}	Forward Transconductance	V _{DS} =15V, I _D =2A	-	3.8	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =480V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±1	uA
Q _g	Total Gate Charge	I _D =2A	-	20	32	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	4.5	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	9	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} =300V	-	11	-	ns
t _r	Rise Time	I _D =2A	-	6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	30	-	ns
t _f	Fall Time	V _{GS} =10V	-	13	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	670	1072	pF
C _{oss}	Output Capacitance	V _{DS} =100V	-	27	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	6	-	pF
R _g	Gate Resistance	f=1.0MHz	-	3.3	6.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =2A, V _{GS} =0V	-	0.8	-	V
t _{rr}	Reverse Recovery Time	I _S =3.2A, V _{GS} =0V	-	65	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	200	-	nC

Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse test
- 3.Ensure that the junction temperature does not exceed T_{Jmax}.
- 4.Starting T_J=25°C , V_{DD}=50V , L=150mH , R_G=25Ω
- 5.I_{SD} ≤ I_D, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C
- 6.Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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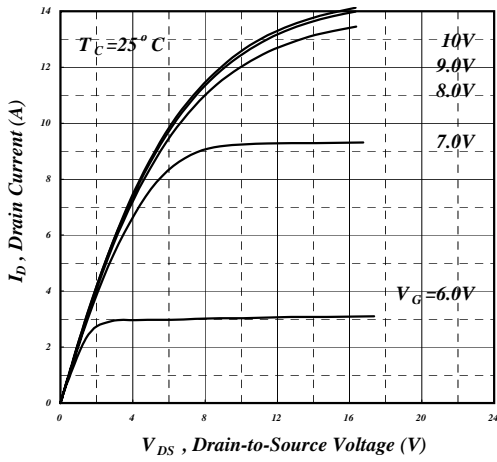


Fig 1. Typical Output Characteristics

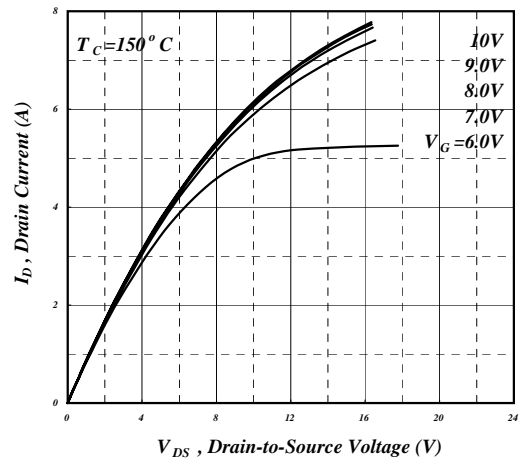


Fig 2. Typical Output Characteristics

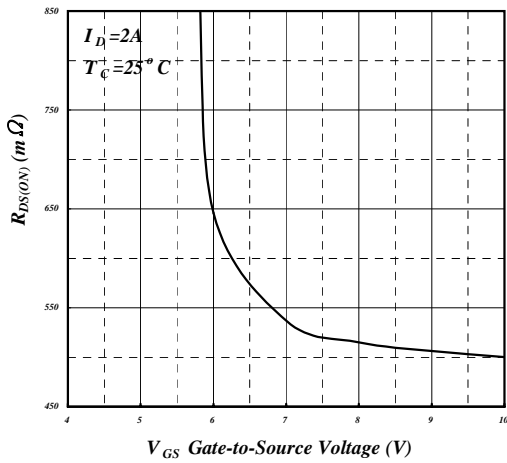


Fig 3. On-Resistance v.s. Gate Voltage

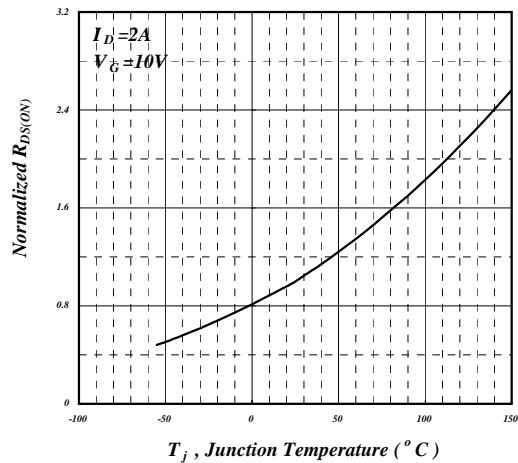


Fig 4. Normalized On-Resistance v.s. Junction Temperature

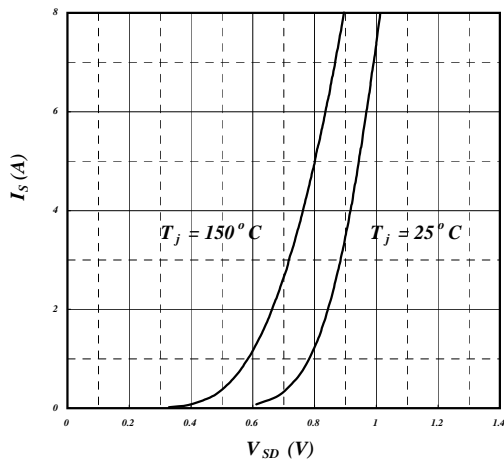


Fig 5. Forward Characteristic of Reverse Diode

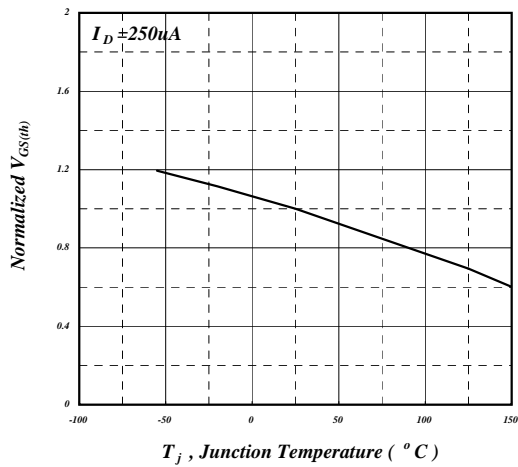


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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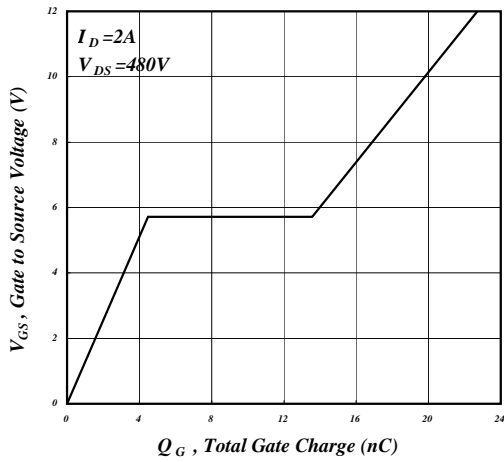


Fig 7. Gate Charge Characteristics

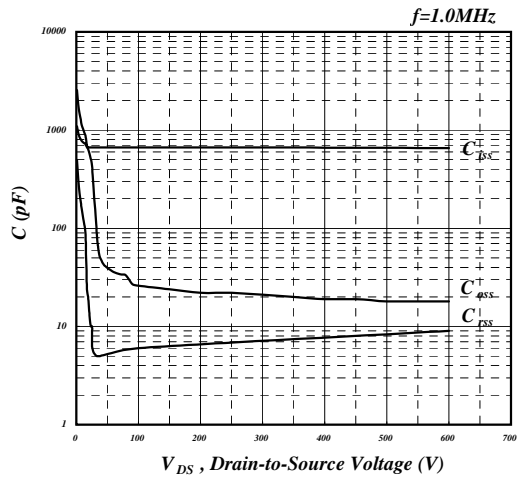


Fig 8. Typical Capacitance Characteristics

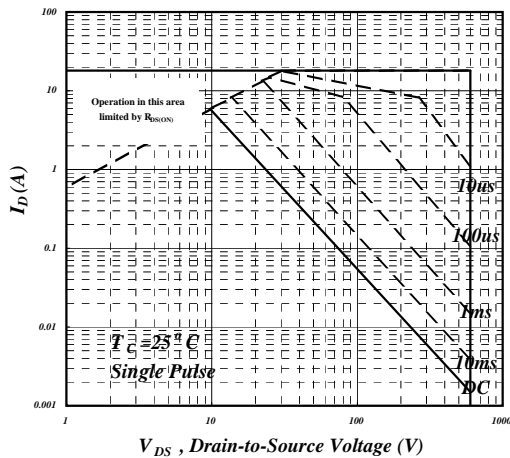


Fig 9. Maximum Safe Operating Area

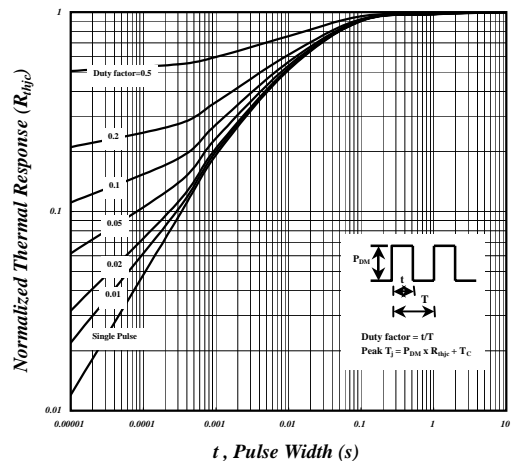


Fig 10. Effective Transient Thermal Impedance

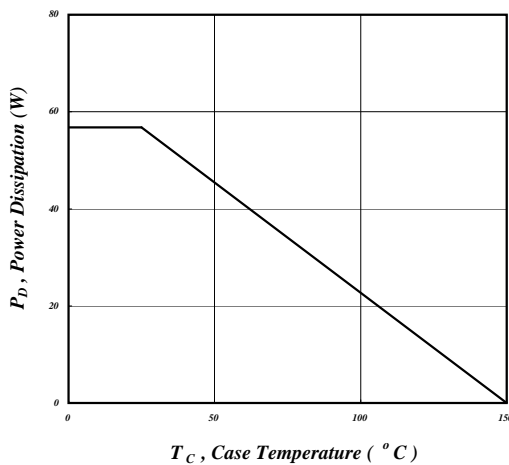


Fig 11. Total Power Dissipation

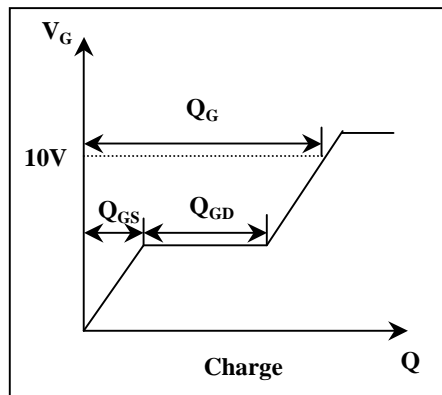
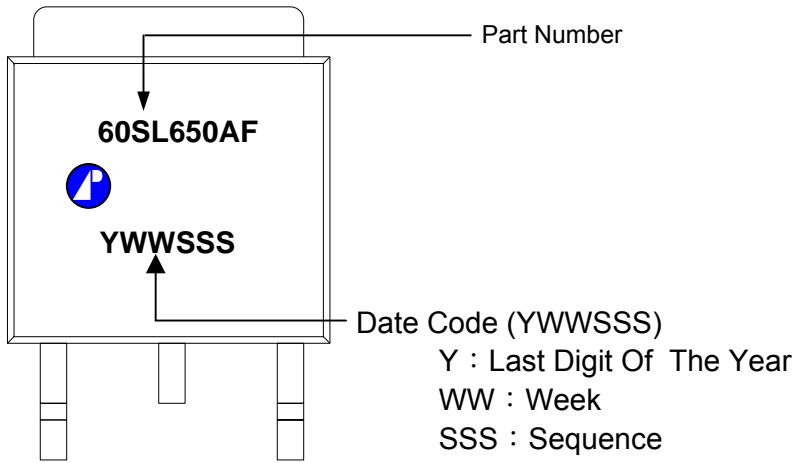


Fig 12. Gate Charge Waveform

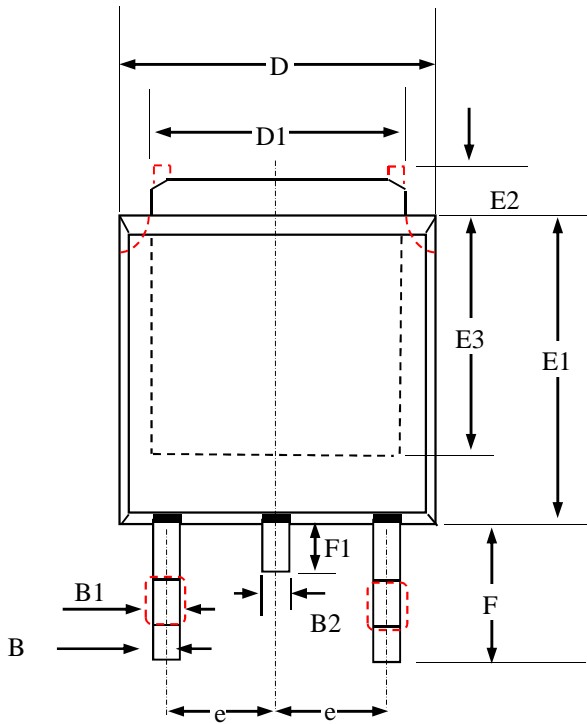


MARKING INFORMATION





Package Outline : TO-252



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A2	2.18	2.30	2.40
A3	0.40	0.50	0.65
B	0.40	0.70	1.00
B1	0.50	0.85	1.20
D	6.00	6.50	6.80
D1	4.80	5.35	5.90
E3	4.00 (ref.)		
F	2.00	2.63	3.05
F1	0.50	0.85	1.20
E1	5.00	5.70	6.30
E2	0.50	1.10	1.80
e	2.3 (ref)		
C	0.35	0.525	0.70
A1	0.00	—	0.25
B2	—	—	1.25
L	0.90	1.34	1.78



1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.
3. Thermal PAD, Body and Pin contour is for reference, it may has little difference by option.



TO-252 FOOTPRINT :

