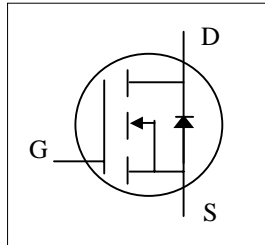
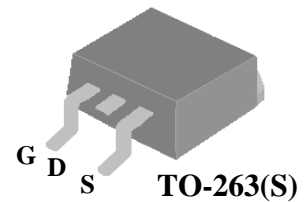




- ▼ 100% R_g & UIS Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV _{DSS}	650V
R _{DS(ON)}	105mΩ
I _D ³	30.8A



Description

AP65SL105AF series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-263 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	+20	V
V _{GS}	Gate-Source Voltage, AC (f > 1Hz)	+30	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ³	30.8	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V ³	19.5	A
I _{DM}	Pulsed Drain Current ¹	90	A
dv/dt	MOSFET dv/dt Ruggedness (V _{DS} = 0 ... 480V)	20	V/ns
P _D @T _C =25°C	Total Power Dissipation	277.8	W
P _D @T _A =25°C	Total Power Dissipation ⁶	3.12	W
E _{AS}	Single Pulse Avalanche Energy ⁴	768	mJ
dv/dt	Peak Diode Recovery dv/dt ⁵	15	V/ns
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	0.45	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁶	40	°C/W



AP65SL105AFS

Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=12.8A$	-	-	105	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	5	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=12.8A$	-	24	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=480V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 1	μA
Q_g	Total Gate Charge	$I_D=12.8A$	-	111	177.6	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=480V$	-	25	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	47	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=300V$	-	26	-	ns
t_r	Rise Time	$I_D=12.8A$	-	33	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	110	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	29	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	4300	6880	pF
C_{oss}	Output Capacitance	$V_{DS}=100V$	-	115	-	pF
C_{riss}	Reverse Transfer Capacitance	$f=1.0MHz$	-	25	-	pF
R_g	Gate Resistance	$f=1.0MHz$	-	4.3	8.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=12.8A, V_{GS}=0V$	-	0.85	-	V
t_{rr}	Reverse Recovery Time	$I_S=19.2A, V_{GS}=0V$	-	120	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	650	-	nC

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse test
3. Ensure that the junction temperature does not exceed T_{jmax} .
4. Starting $T_j=25^\circ\text{C}$, $V_{DD}=50V$, $L=150mH$, $R_G=25\Omega$
5. $I_{SD} \leq I_D$, $V_{DD} \leq BV_{DSS}$, starting $T_j = 25^\circ\text{C}$
6. Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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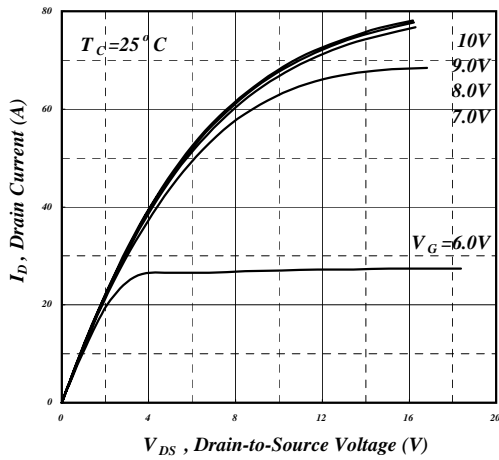


Fig 1. Typical Output Characteristics

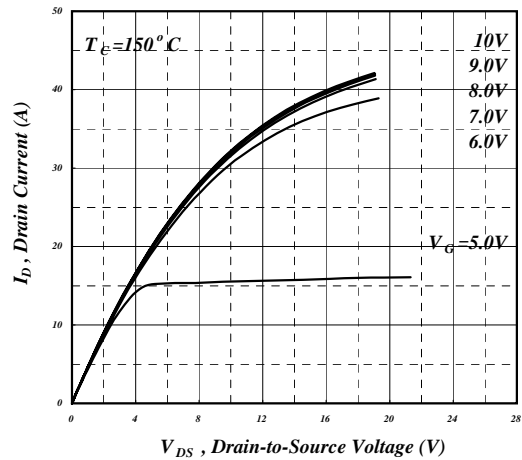


Fig 2. Typical Output Characteristics

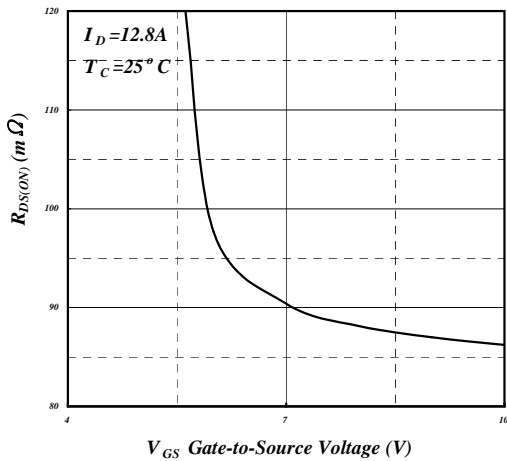


Fig 3. On-Resistance v.s. Gate Voltage

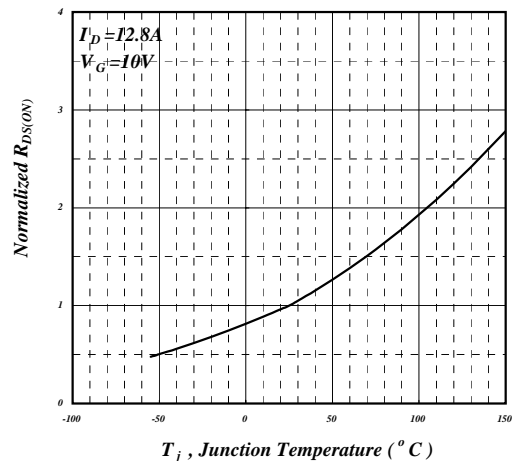


Fig 4. Normalized On-Resistance v.s. Junction Temperature

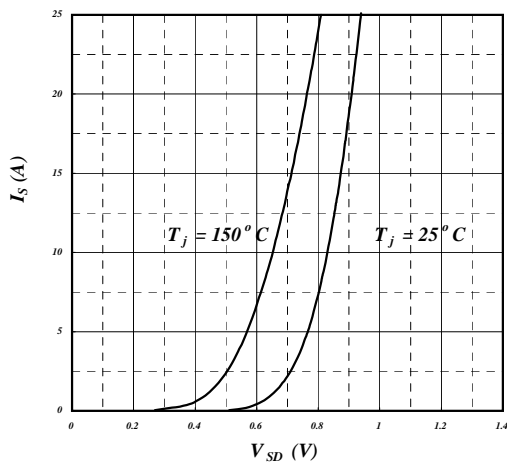


Fig 5. Forward Characteristic of Reverse Diode

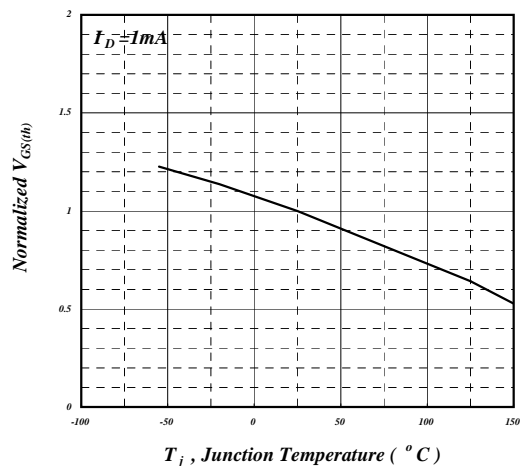


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

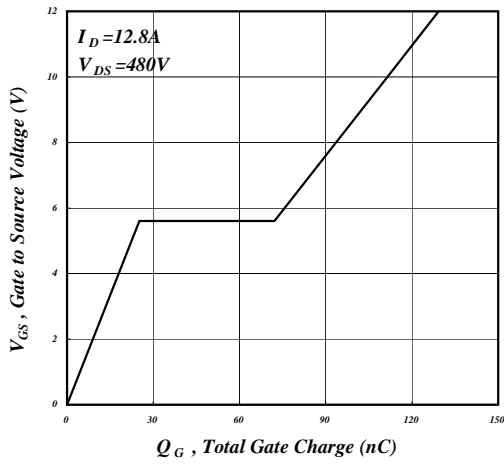


Fig 7. Gate Charge Characteristics

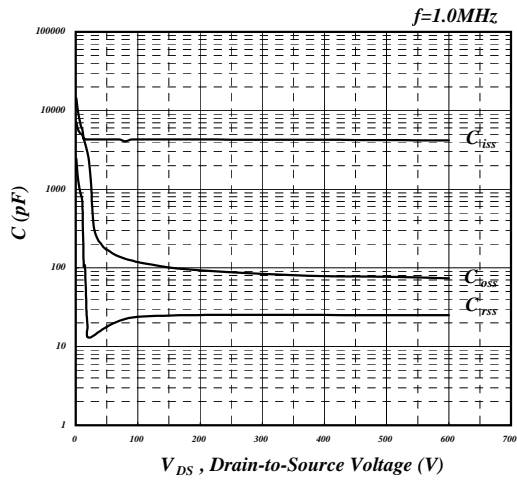


Fig 8. Typical Capacitance Characteristics

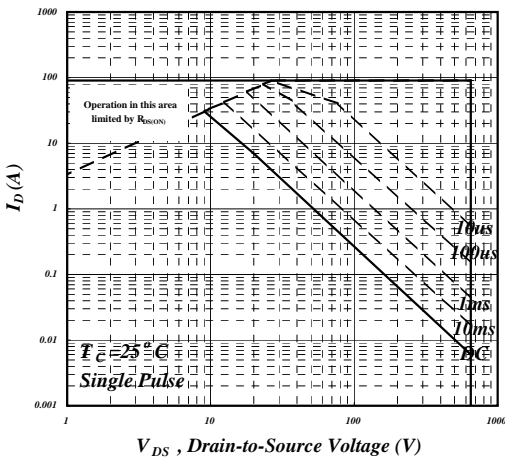


Fig 9. Maximum Safe Operating Area

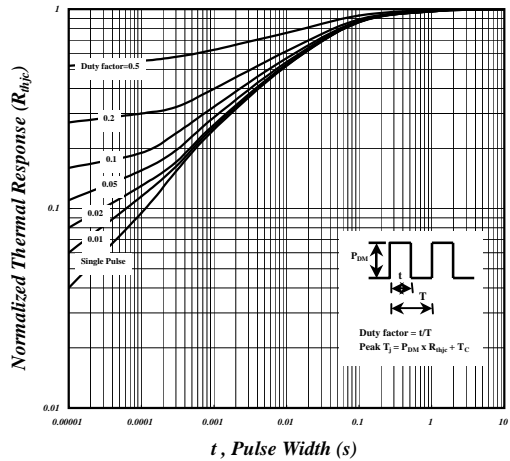


Fig 10. Effective Transient Thermal Impedance

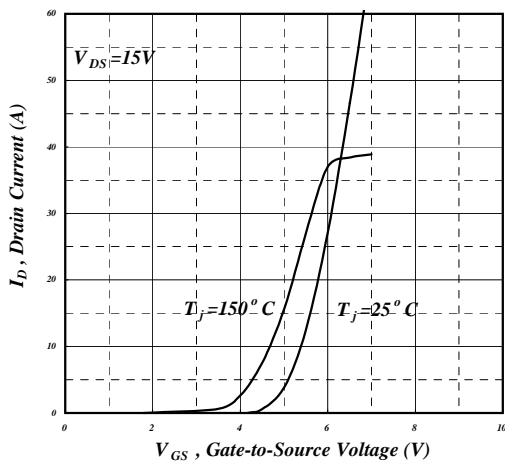


Fig 11. Transfer Characteristics

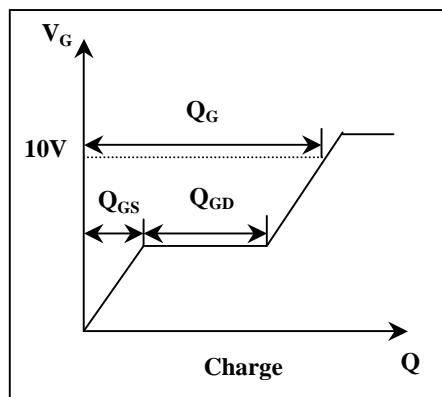


Fig 12. Gate Charge Waveform

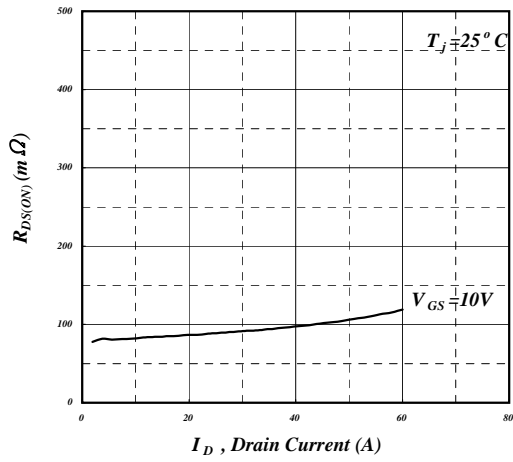


Fig 13. Typ. Drain-Source on State Resistance

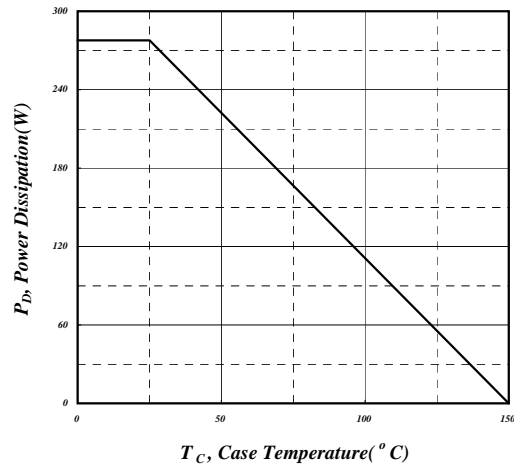
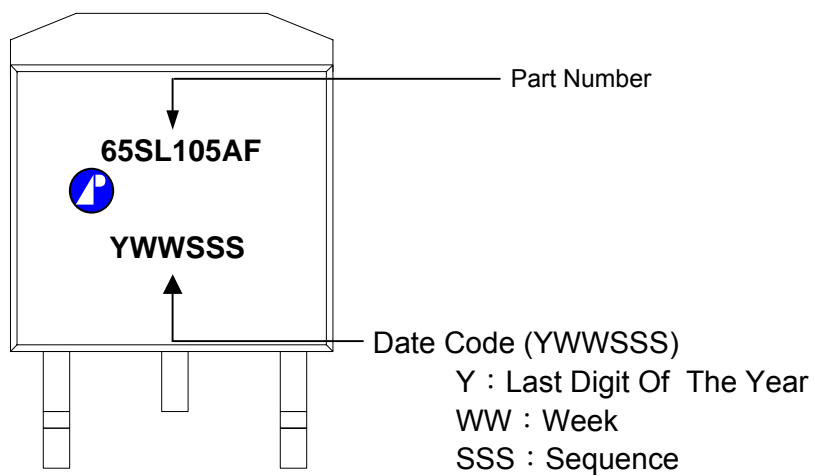


Fig 14. Total Power Dissipation



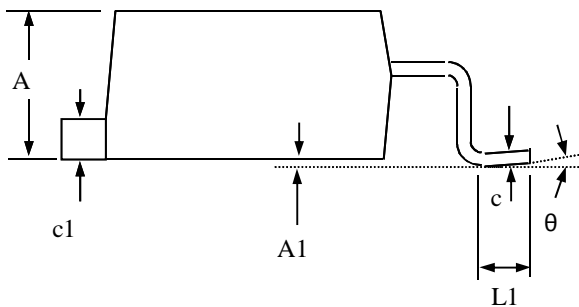
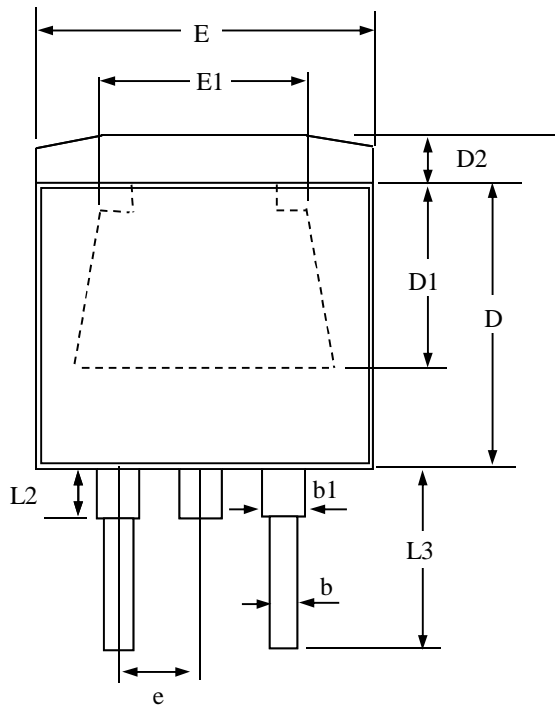
AP65SL105AFS

MARKING INFORMATION





Package Outline : TO-263



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.00	4.75	5.20
A1	0.00	0.15	0.30
b	0.50	0.90	1.10
b1	1.07	1.27	1.47
c	0.30	0.55	0.80
c1	1.10	1.40	1.70
D	8.30	9.05	9.80
D1	5.10(ref)		
D2	1.27(ref)		
E	9.50	10.10	10.70
E1	7.00~9.00(ref)		
e	2.04	2.54	3.04
L1	2.54(ref)		
L2	1.5 (ref)		
L3	3.50	4.50	5.50
θ	0°	-----	8°

1.All Dimensions Are in Millimeters.

2.Dimension Does Not Include Mold Protrusions.



TO-263 FOOTPRINT :

