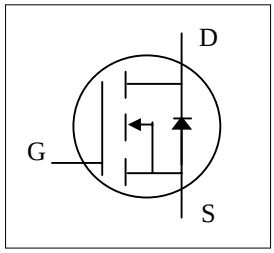
AP65SL190DIN

Halogen-Free Product

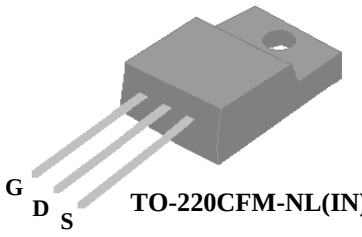
Advanced Power Electronics Corp.

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **100% R_g & UIS Test**
- ▼ **Low t_{rr} / Q_{rr}**
- ▼ **Simple Drive Requirement**
- ▼ **RoHS Compliant & Halogen-Free**



BV_{DSS}	650V
$R_{DS(ON)}$	0.19Ω
I_D[3,4]	20A



TO-220CFM-NL(IN)

Description

AP65SL190D series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	±20	V
V_{GS}	Gate-Source Voltage, AC (f > 1Hz)	±30	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[3,4]	20	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V[3,4]	12.3	A
I_{DM}	Pulsed Drain Current[1]	48	A
dv/dt	MOSFET dv/dt Ruggedness (V_{DS} = 0 …400V)	20	V/ns
P_D@T_C=25℃	Total Power Dissipation	34.7	W
P_D@T_A=25℃	Total Power Dissipation	1.92	W
E_{AS}	Single Pulse Avalanche Energy[5]	300	mJ
dv/dt	Peak Diode Recovery dv/dt[6]	15	V/ns
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.6	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	650	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=6.2A	-	-	0.19	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	5	V
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D=7.5A	-	12	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=480V, V_{GS}=0V	-	-	100	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±1	uA
Q_g	Total Gate Charge	I_D=7.5A	-	58	92.8	nC
Q_{gs}	Gate-Source Charge	V_{DS}=480V	-	13	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	26	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=300V	-	17	-	ns
t_r	Rise Time	I_D=7.5A	-	19	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	57	-	ns
t_f	Fall Time	V_{GS}=10V	-	16	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	2070	3312	pF
C_{oss}	Output Capacitance	V_{DS}=100V	-	60	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	5	-	pF
R_g	Gate Resistance	f=1.0MHz	-	4.1	8.2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=6.2A, V_{GS}=0V	-	0.8	-	V
t_{rr}	Reverse Recovery Time	I_S=11A, V_{GS}=0V	-	155	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	1.2	-	μC

Notes:

Notes:

1.Pulse width limited by max. junction temperature.

2.Pulse test

3.Limited by max. junction temperature. Maximum duty cycle D=0.75

4.Ensure that the junction temperature does not exceed $T_{Jmax.}$.

5.Starting T_j=25°C , V_{DD}=90V , L=150mH , R_G=25Ω, V_{GS}=10V

6.I_{SD} ≦ I_D, V_{DD} ≦ BV_{DSS}, starting T_J = 25°C

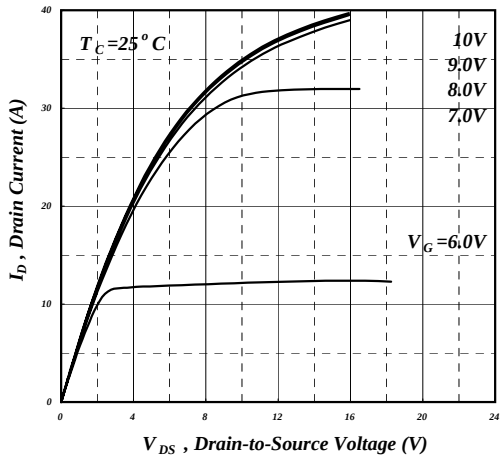


Fig 1. Typical Output Characteristics

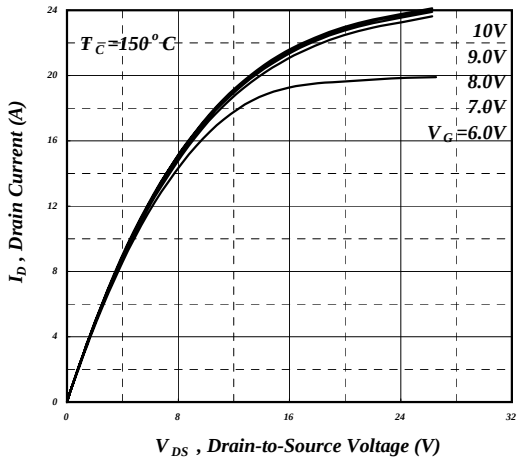


Fig 2. Typical Output Characteristics

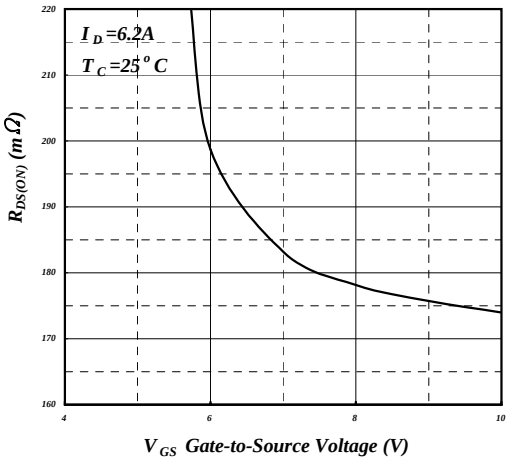


Fig 3. On-Resistance v.s. Gate Voltage

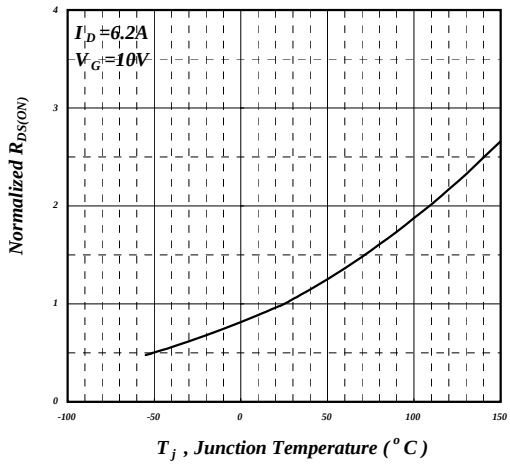


Fig 4. Normalized On-Resistance v.s. Junction Temperature

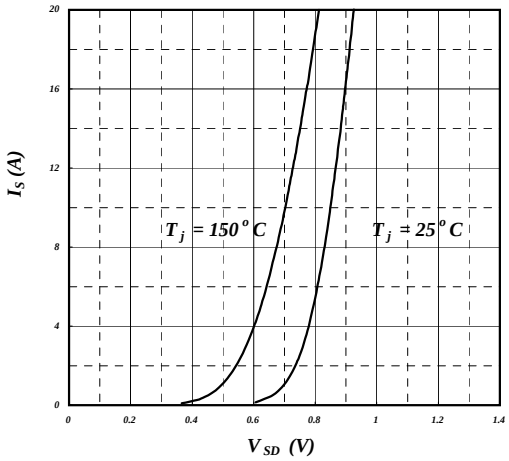


Fig 5. Forward Characteristic of Reverse Diode

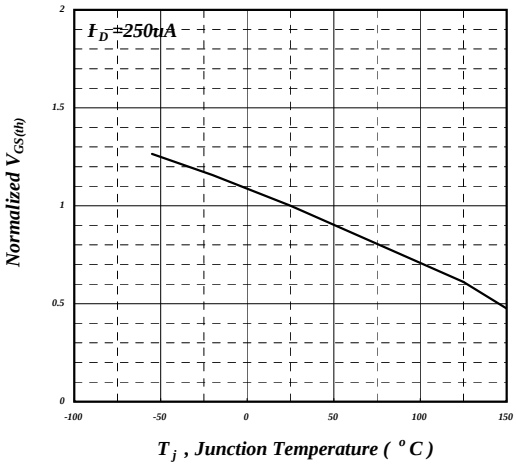


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

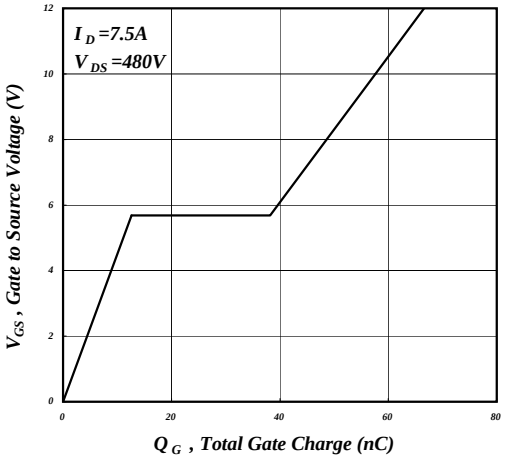


Fig 7. Gate Charge Characteristics

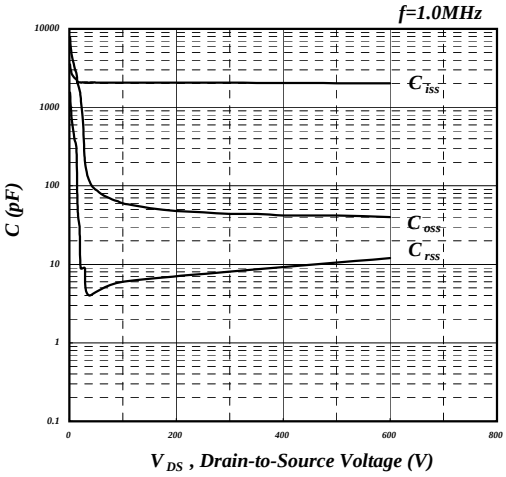


Fig 8. Typical Capacitance Characteristics

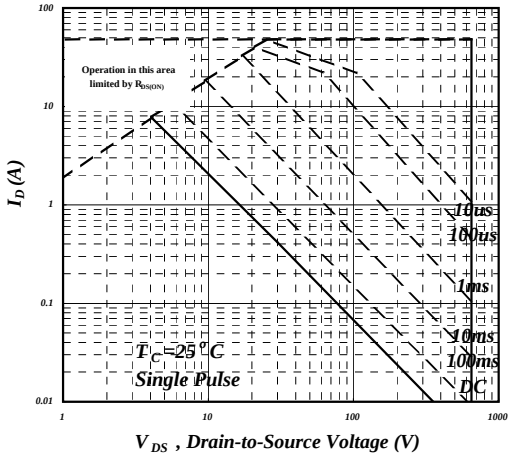


Fig 9. Maximum Safe Operating Area

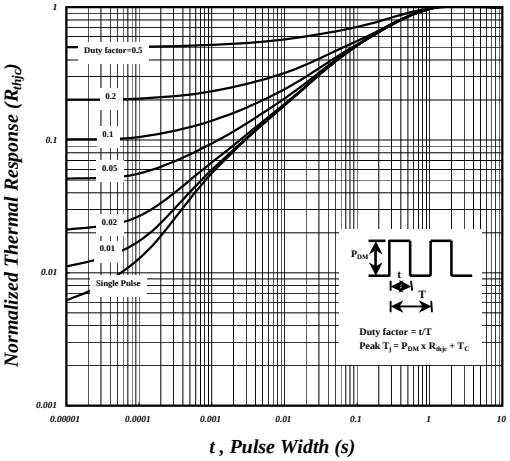


Fig10. Effective Transient Thermal Impedance

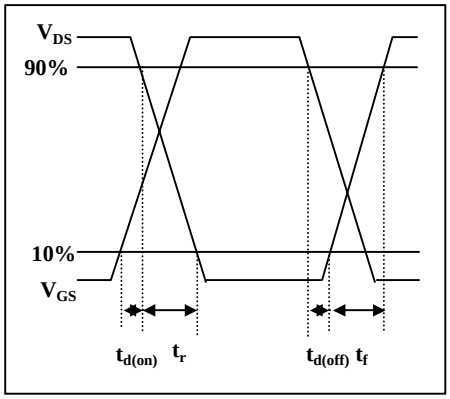


Fig 11. Switching Time Waveform

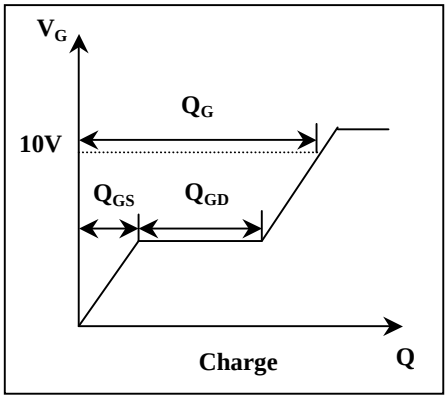


Fig 12. Gate Charge Waveform

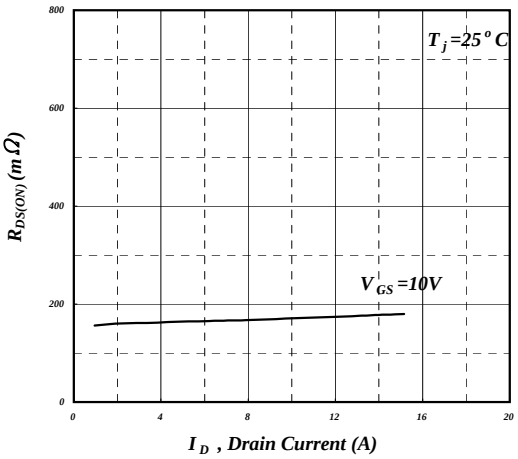


Fig 13. Typ. Drain-Source on State Resistance

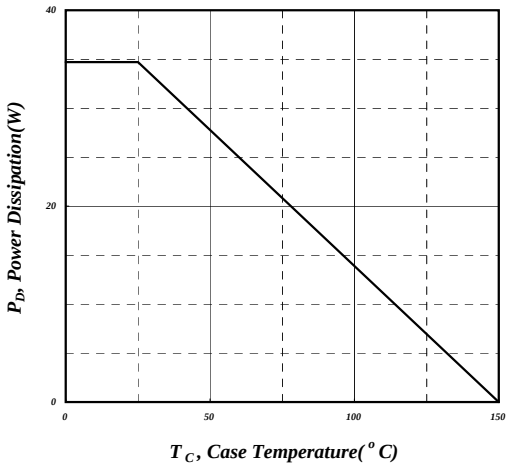
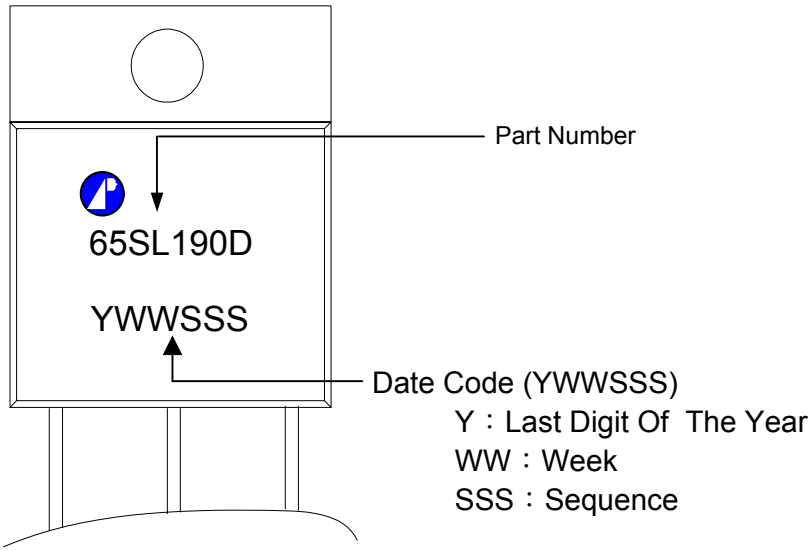
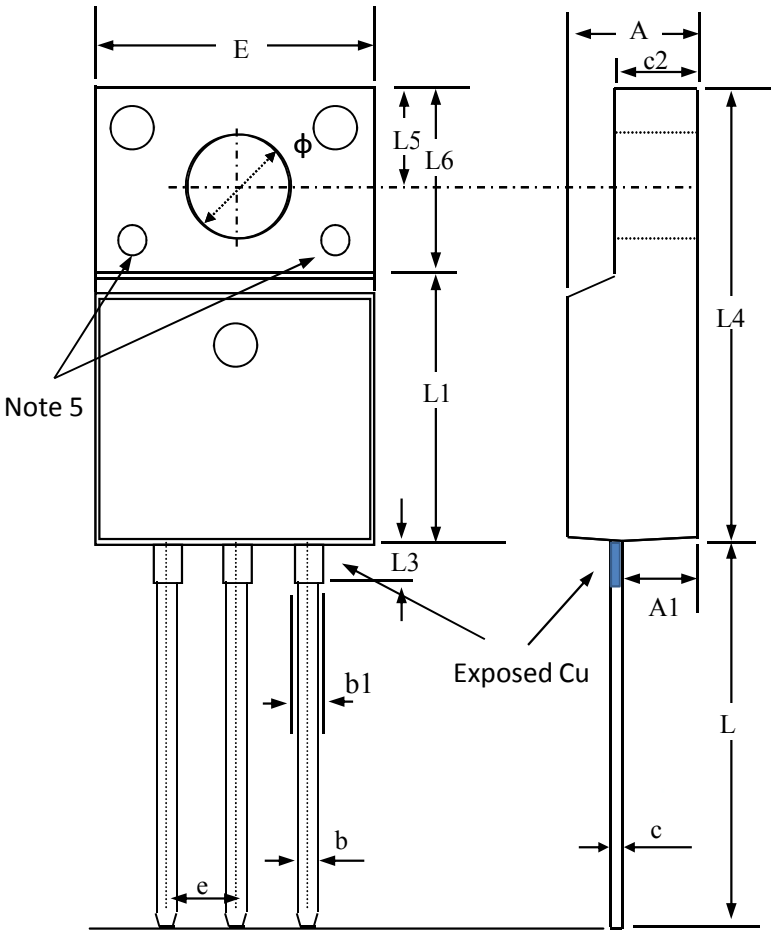


Fig 14. Total Power Dissipation

MARKING INFORMATION



Package Outline : TO-220CFM-NL



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.50	2.60	2.70
b	0.60	0.70	0.80
b1	0.60	0.80	0.90
c	0.45	0.50	0.60
c2	2.50	2.70	2.90
E	9.70	10.00	10.30
L	13.40	13.60	13.80
L1		8.5 (ref.)	
L3	1.00	1.10	1.20
L4	14.70	15.00	15.30
L5	2.90	3.00	3.10
L6	6.30	6.50	6.70
φ	3.00	3.20	3.40
e	2.60 (BSC)		

1.All Dimensions Are in Millimeters.

2. Package body sizes exclude mold flash and burrs mold flash should be less than 6 mil.

3. Stand off 1.10mm.

4. Ejector pin on package hole: φ1.5 dep 0.1mm

5. Potting process option for these two holes

Draw No. M1-I3NL-G-v00

TO-220CFM-NL FOOTPRINT：