

AP65SL600AIN

Halogen-Free Product

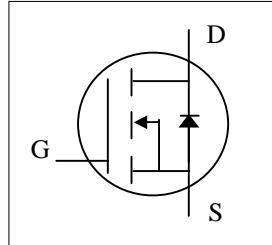


**Advanced Power
Electronics Corp.**

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% R_g & UIS Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

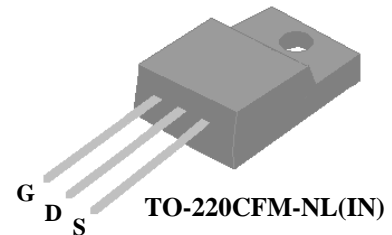


V _{DS} @ T _{j,max.}	700V
R _{DS(ON)}	0.6 Ω
I _D	7A

Description

AP65SL600A series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.



Absolute Maximum Ratings @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ^{3,4}	7	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V ^{3,4}	4.4	A
I _{DM}	Pulsed Drain Current ¹	18	A
dv/dt	MOSFET dv/dt Ruggedness (V _{DS} = 0 ...400V)	50	V/ns
P _D @T _C =25°C	Total Power Dissipation	27.8	W
P _D @T _A =25°C	Total Power Dissipation	1.92	W
E _{AS}	Single Pulse Avalanche Energy ⁵	36.7	mJ
dv/dt	Peak Diode Recovery dv/dt ⁶	15	V/ns
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	4.5	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient	65	°C/W



AP65SL600AIN

Electrical Characteristics @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	650	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =2A	-	-	0.6	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	5	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =2A	-	5	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =480V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =2A	-	20	32	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	4	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	9	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} =300V	-	8	-	ns
t _r	Rise Time	I _D =2A	-	20	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	28	-	ns
t _f	Fall Time	V _{GS} =10V	-	23	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	740	1184	pF
C _{oss}	Output Capacitance	V _{DS} =100V	-	28	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	2	-	pF
R _g	Gate Resistance	f=1.0MHz	-	3.8	7.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =2A, V _{GS} =0V	-	0.8	-	V
t _{rr}	Reverse Recovery Time	I _S =7A, V _{GS} =0V	-	280	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=50A/μs	-	1.8	-	μC

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse test
3. Limited by max. junction temperature. Maximum duty cycle D=0.75
4. Ensure that the junction temperature does not exceed T_{Jmax}.
5. Starting T_J=25°C, V_{DD}=50V, L=150mH, R_G=25Ω
6. I_{SD} ≤ I_D, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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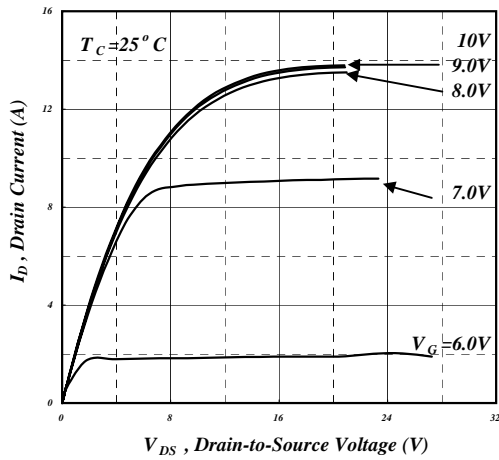


Fig 1. Typical Output Characteristics

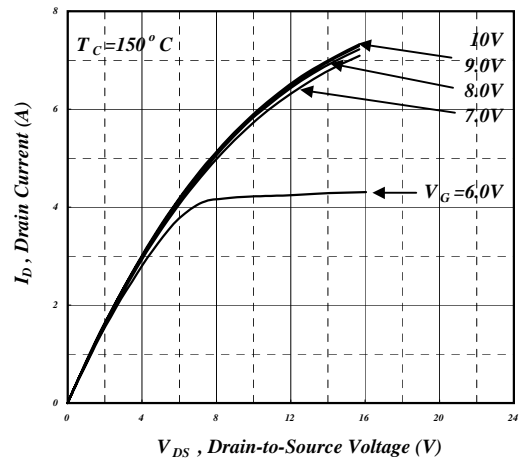


Fig 2. Typical Output Characteristics

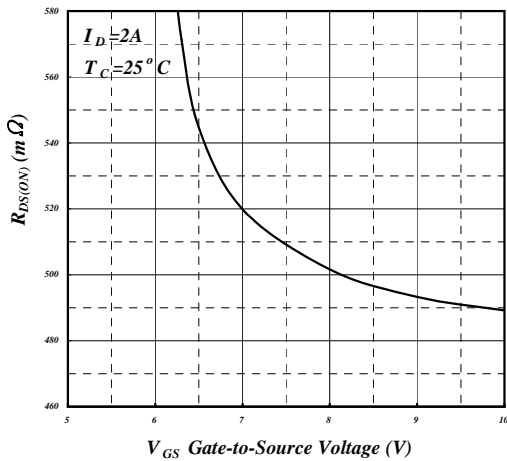


Fig 3. On-Resistance v.s. Gate Voltage

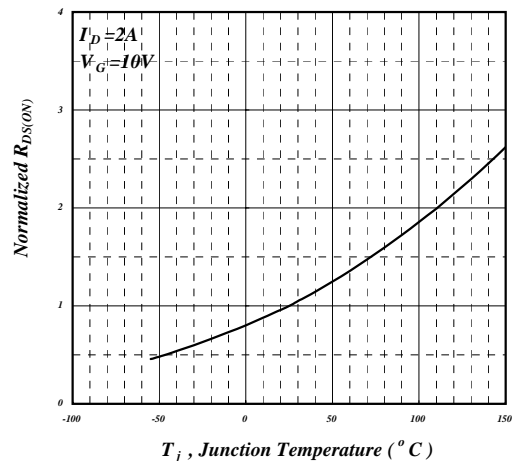


Fig 4. Normalized On-Resistance v.s. Junction Temperature

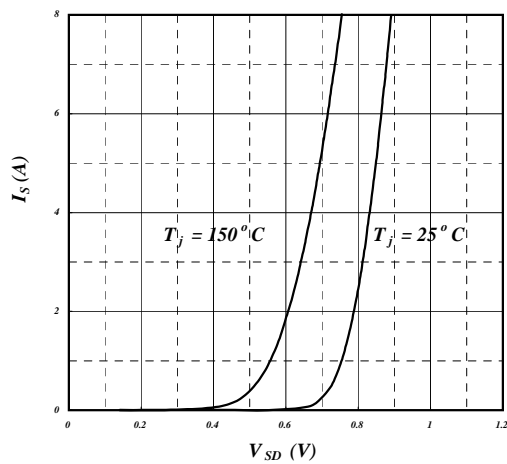


Fig 5. Forward Characteristic of Reverse Diode

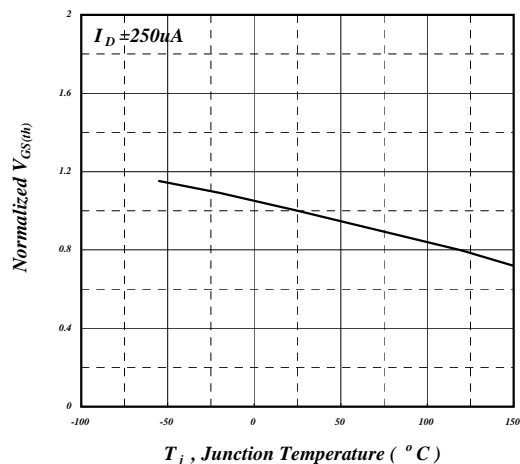


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

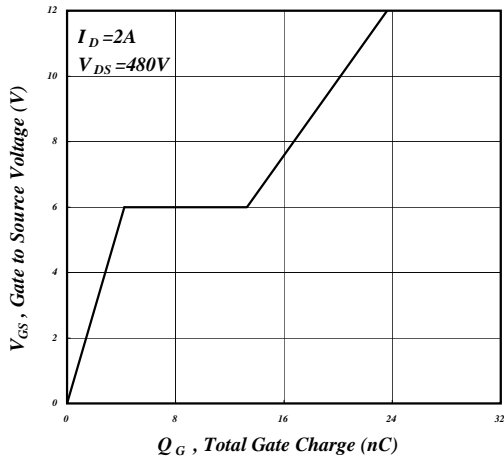


Fig 7. Gate Charge Characteristics

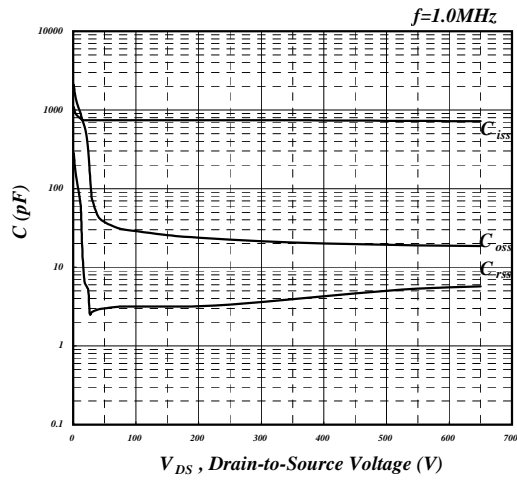


Fig 8. Typical Capacitance Characteristics

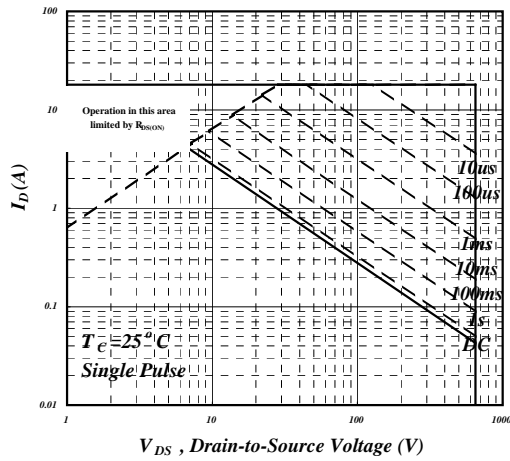


Fig 9. Maximum Safe Operating Area

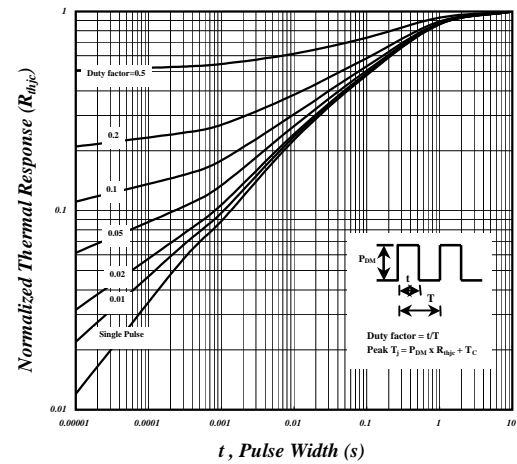


Fig 10. Effective Transient Thermal Impedance

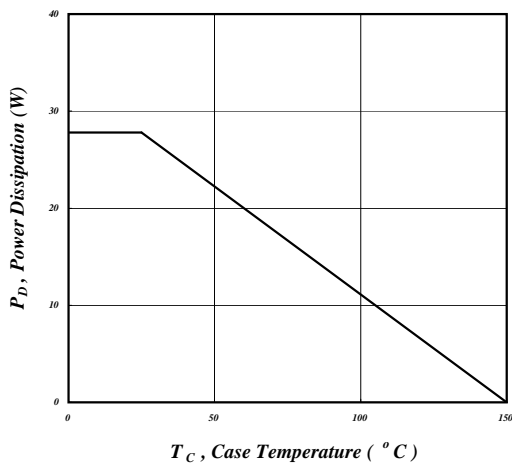


Fig 11. Total Power Dissipation

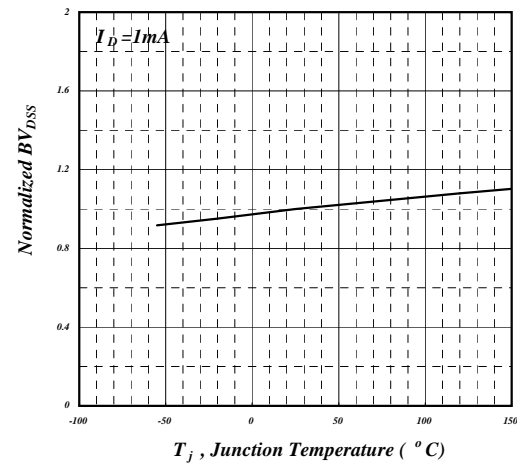
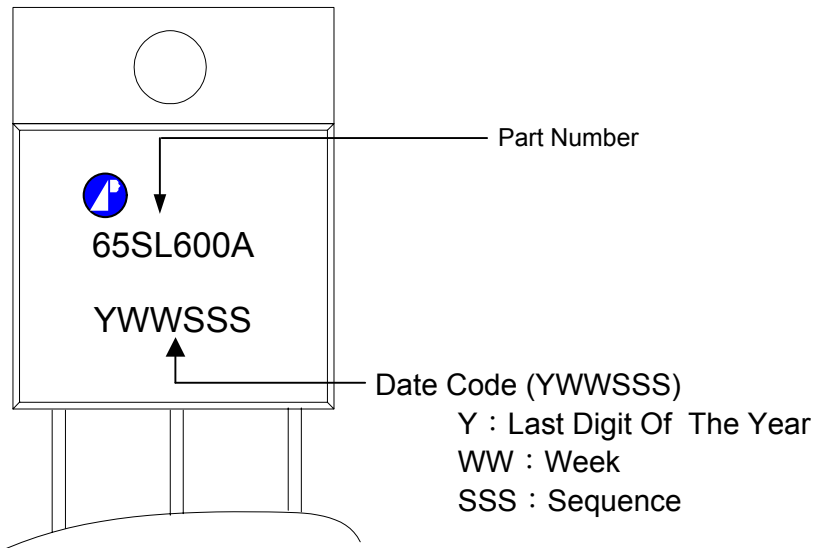


Fig 12. Normalized BV_{DS} v.s. Junction Temperature

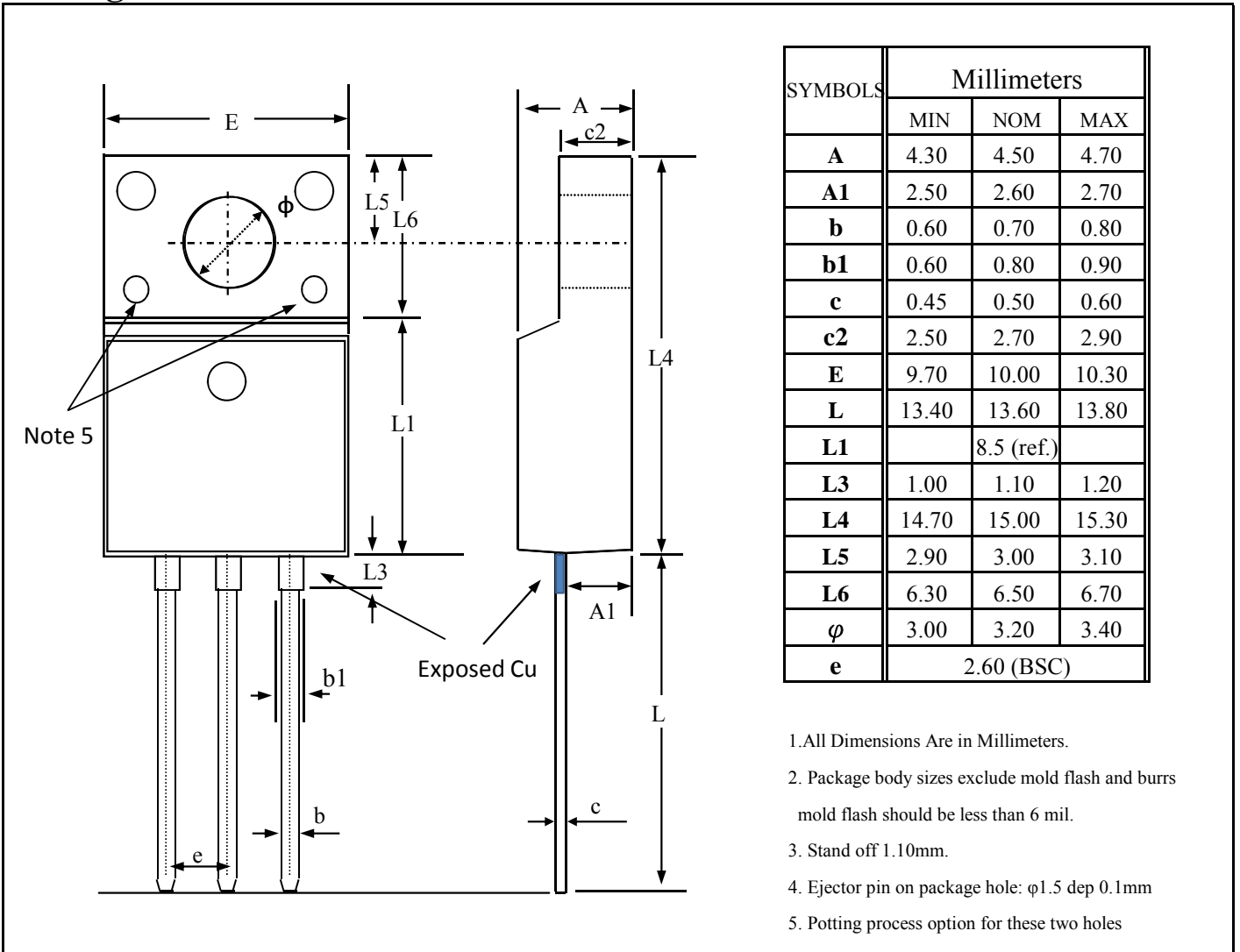


MARKING INFORMATION





Package Outline : TO-220CFM-NL



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.50	2.60	2.70
b	0.60	0.70	0.80
b1	0.60	0.80	0.90
c	0.45	0.50	0.60
c2	2.50	2.70	2.90
E	9.70	10.00	10.30
L	13.40	13.60	13.80
L1		8.5 (ref.)	
L3	1.00	1.10	1.20
L4	14.70	15.00	15.30
L5	2.90	3.00	3.10
L6	6.30	6.50	6.70
φ	3.00	3.20	3.40
e	2.60 (BSC)		

1. All Dimensions Are in Millimeters.
2. Package body sizes exclude mold flash and burrs
mold flash should be less than 6 mil.
3. Stand off 1.10mm.
4. Ejector pin on package hole: $\phi 1.5$ dep 0.1mm
5. Potting process option for these two holes



TO-220CFM-NL FOOTPRINT :

