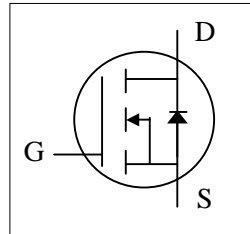




- ▼ Simple Drive Requirement
- ▼ Lower On-resistance
- ▼ RoHS Compliant & Halogen-Free

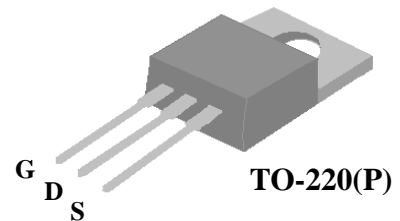


$BV_{DSS}$	75V
$R_{DS(ON)}$	3.4m $\Omega$
$I_D$	210A

## Description

AP97T07A series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.



## Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	75	V
$V_{GS}$	Gate-Source Voltage	+20	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current (Chip)	210	A
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	120	A
$I_D @ T_C=100^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	120	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	480	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	277.8	W
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	0.45	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$



# AP97T07AGP-HF

## Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	75	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=60A$	-	-	3.4	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	5	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=60A$	-	100	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=75V, V_{GS}=0V$	-	-	10	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge	$I_D=40A$	-	160	256	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=60V$	-	25	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	90	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=40V$	-	115	-	ns
$t_r$	Rise Time	$I_D=40A$	-	330	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=25\Omega$	-	260	-	ns
$t_f$	Fall Time	$V_{GS}=10V$	-	350	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	6400	10240	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	1040	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	720	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	2.2	4.4	$\Omega$

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=40A, V_{GS}=0V$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_S=10A, V_{GS}=0V$	-	70	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	175	-	nC

### Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Package limitation current is 120A.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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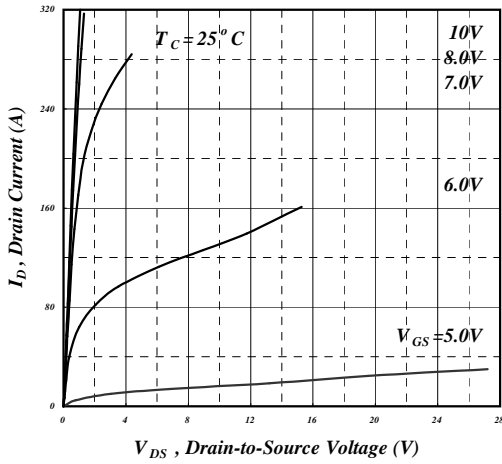


Fig 1. Typical Output Characteristics

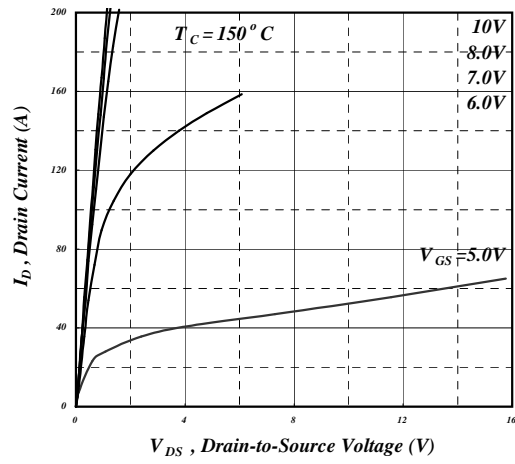


Fig 2. Typical Output Characteristics

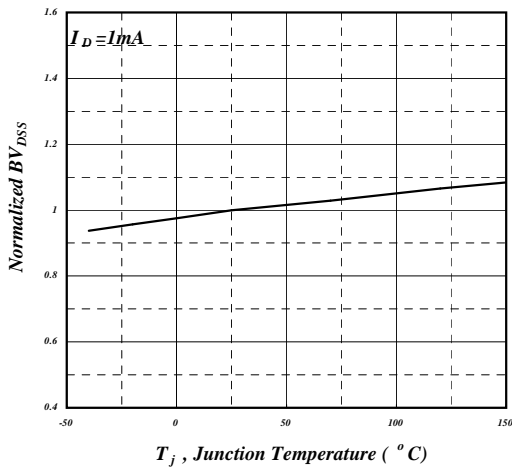


Fig 3. Normalized  $BV_{DSS}$  v.s. Junction Temperature

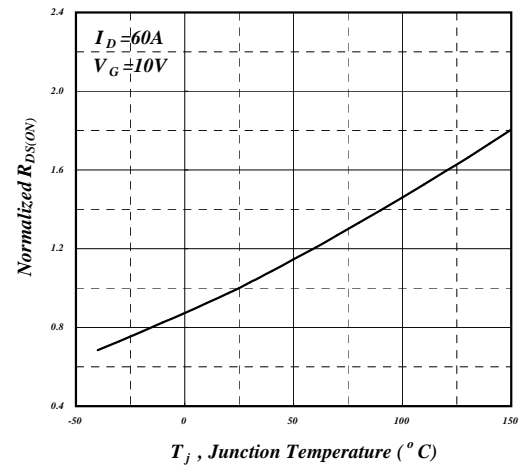


Fig 4. Normalized On-Resistance v.s. Junction Temperature

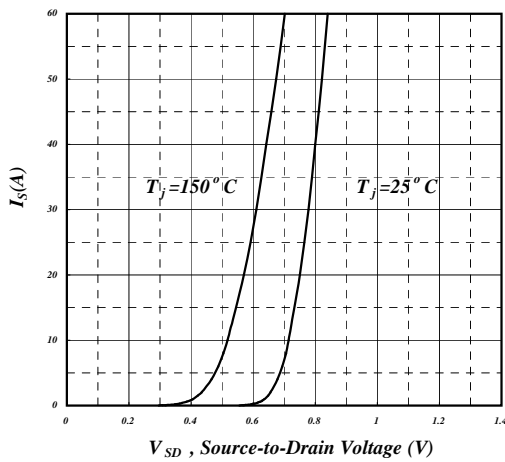


Fig 5. Forward Characteristic of Reverse Diode

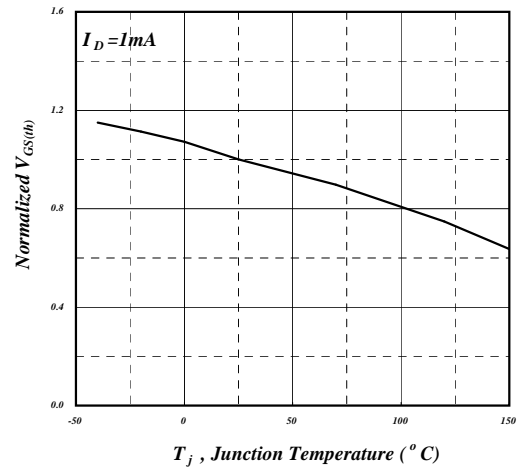


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



# AP97T07AGP-HF

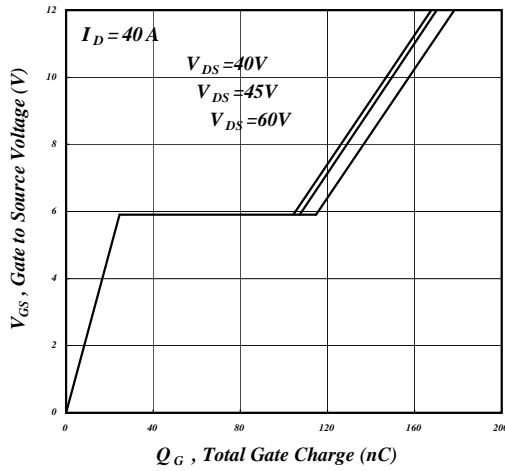


Fig 7. Gate Charge Characteristics

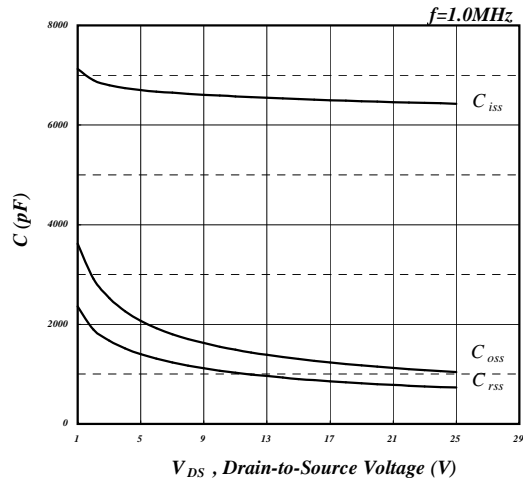


Fig 8. Typical Capacitance Characteristics

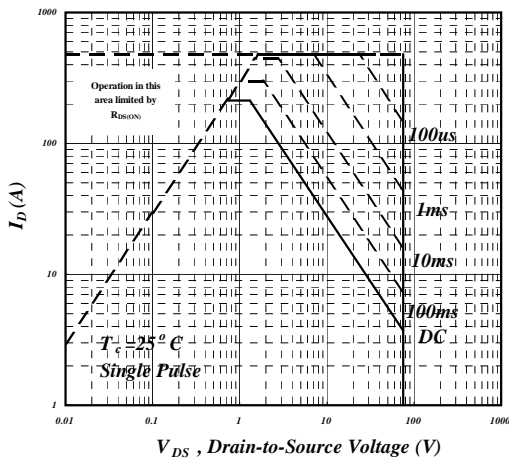


Fig 9. Maximum Safe Operating Area

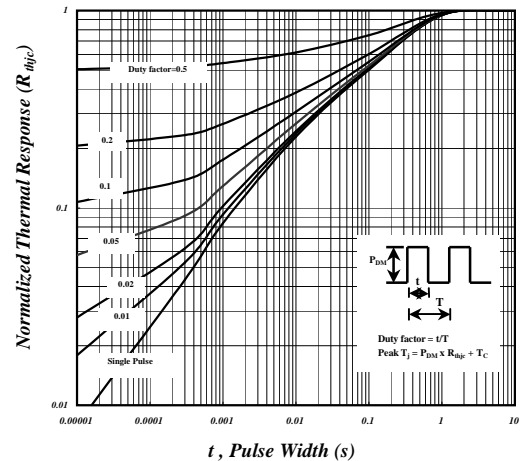


Fig 10. Effective Transient Thermal Impedance

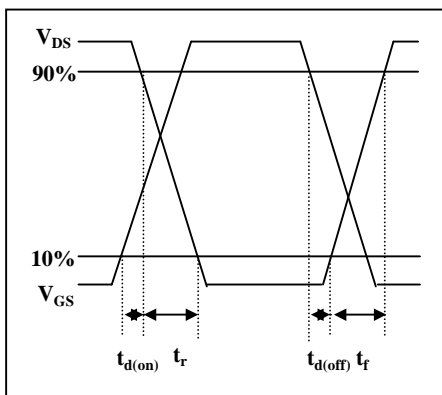


Fig 11. Switching Time Waveform

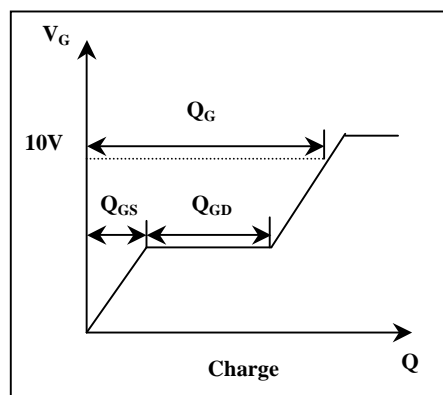
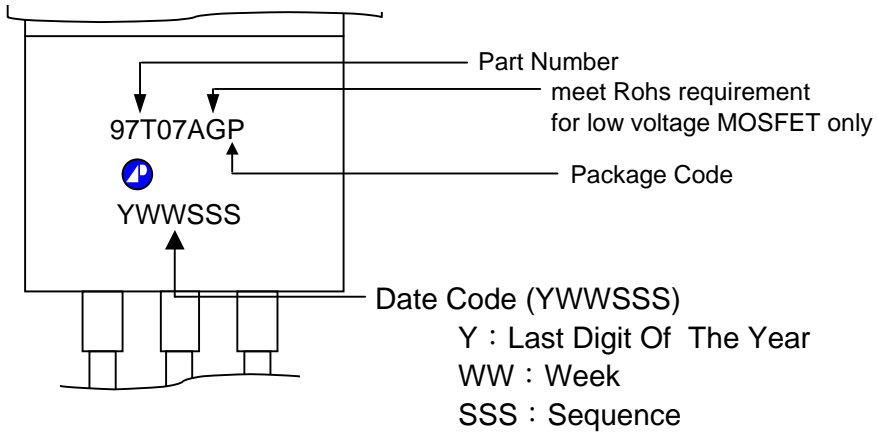


Fig 12. Gate Charge Waveform

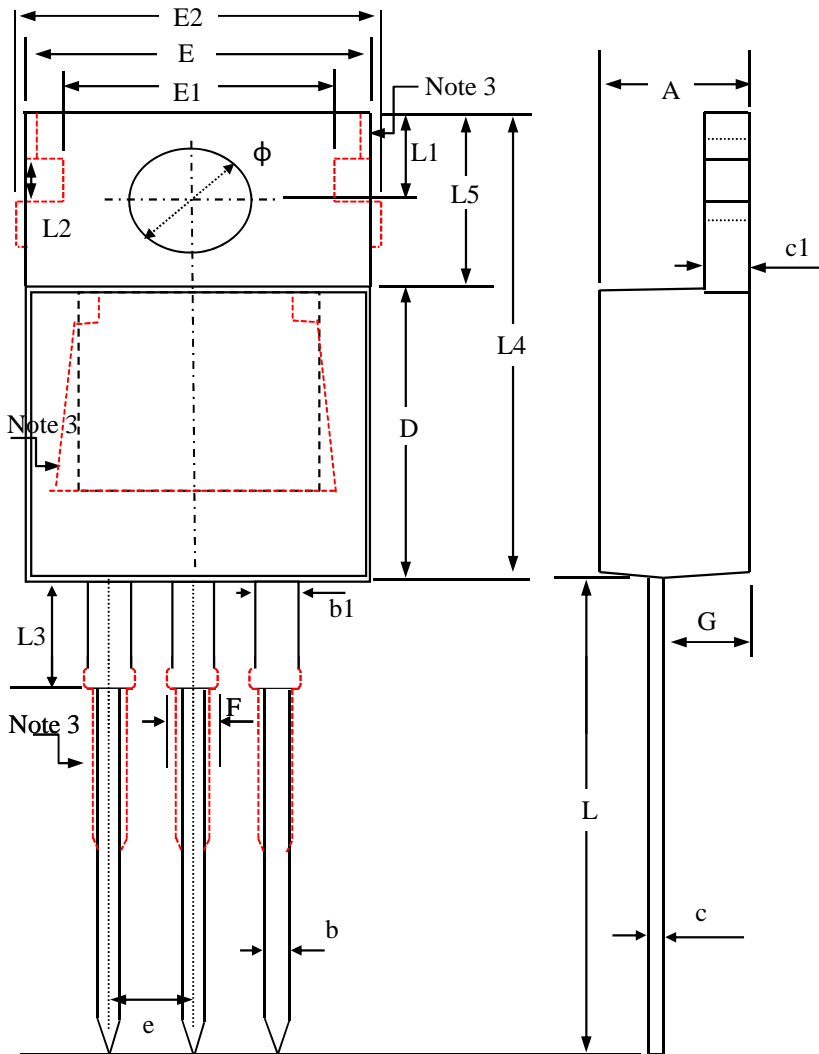


## MARKING INFORMATION





## Package Outline : TO-220



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.20	4.50	4.80
b	0.60	0.80	1.00
b1	1.10	1.38	1.80
c	0.30	0.48	0.65
c1	1.10	1.30	1.50
E	9.70	10.00	10.40
E1	7.40	8.30	9.20
e	2.54 (ref.)		
L	12.70	13.60	14.50
L1	2.50	2.75	3.00
L2	1.00	1.40	1.80
L3	2.60	3.35	4.10
L4	14.30	15.15	16.00
L5	6.00	6.40	6.80
$\phi$	3.40	3.70	4.00
D	8.30	8.85	9.40
F	1.20	1.41	1.85
G	2.20	2.60	3.00
E2	—	—	11.50

Note:

- 1.All Dimensions Are in Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.



**TO-220 FOOTPRINT :**

