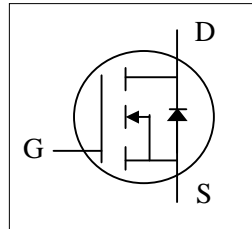




- ▼ Low Gate Charge
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

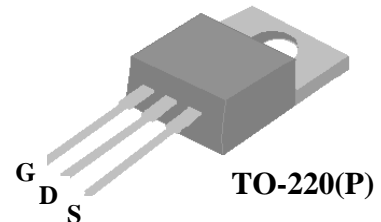
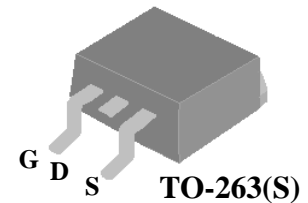


BV_{DSS}	60V
$R_{DS(ON)}$	18m Ω
I_D	60A

Description

AP9972 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-263 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance. The through-hole version (AP9972GP) are available for low-profile applications.



Absolute Maximum Ratings @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	+25	V
$I_D @ T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}$	60	A
$I_D @ T_C=100^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}$	38	A
I_{DM}	Pulsed Drain Current ¹	230	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	89	W
	Linear Derating Factor	0.7	W/ $^\circ\text{C}$
E_{AS}	Single Pulse Avalanche Energy ³	45	mJ
I_{AR}	Avalanche Current ³	30	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.4	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁴	40	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$



Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^{\circ}\text{C}, I_D=1\text{mA}$	-	0.06	-	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=35A$	-	-	18	$m\Omega$
		$V_{GS}=4.5V, I_D=25A$	-	-	22	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=35A$	-	55	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=60V, V_{GS}=0V$	-	-	10	μA
	Drain-Source Leakage Current ($T_j=125^{\circ}\text{C}$)	$V_{DS}=48V, V_{GS}=0V$	-	-	250	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_D=35A$	-	32	51	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=48V$	-	8	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	20	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=30V$	-	11	-	ns
t_r	Rise Time	$I_D=35A$	-	58	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	45	-	ns
t_f	Fall Time	$R_D=0.86\Omega$	-	80	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	3170	5070	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	280	-	pF
C_{riss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	230	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1.7	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=35A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_S=35A, V_{GS}=0V,$	-	50	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	48	-	nC

Notes:

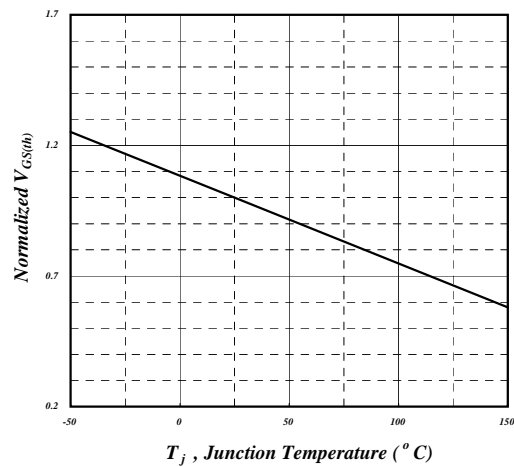
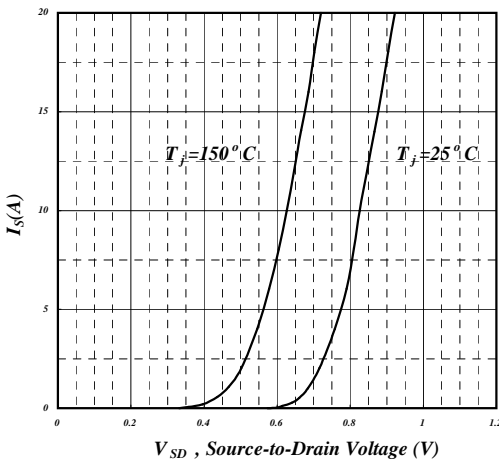
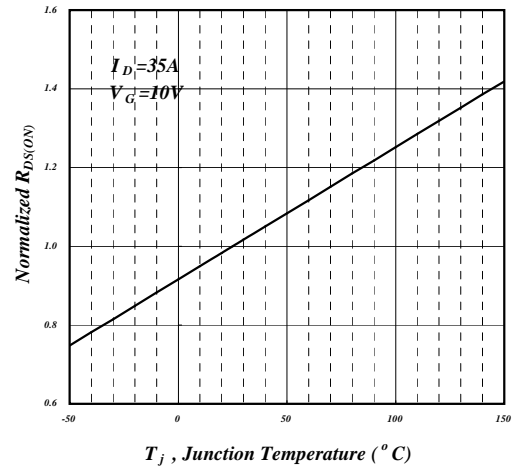
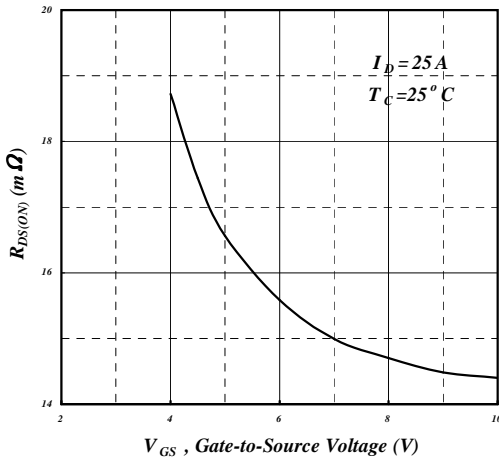
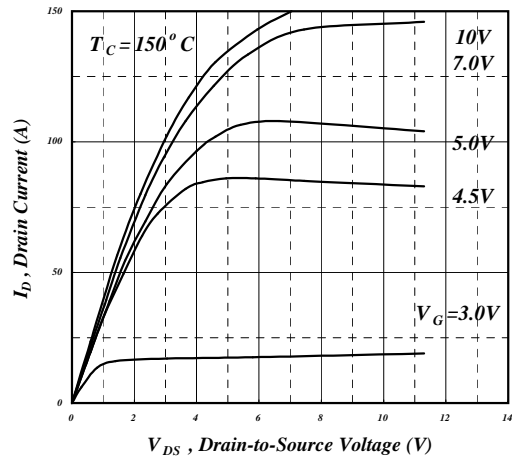
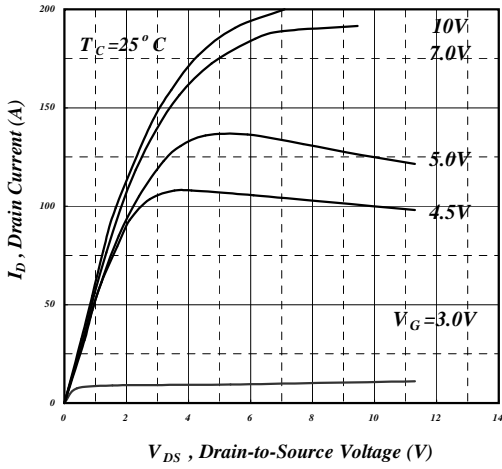
1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=30V$, $L=100\mu H$, $R_G=25\Omega$, $I_{AS}=30A$.
4. Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



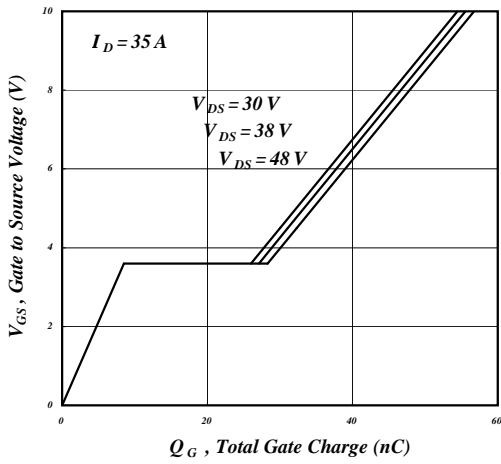


Fig 7. Gate Charge Characteristics

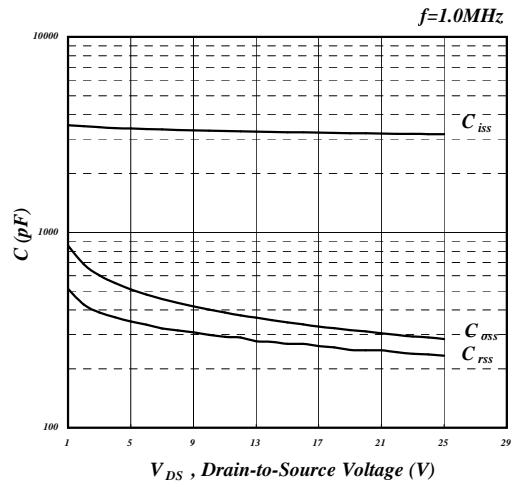


Fig 8. Typical Capacitance Characteristics

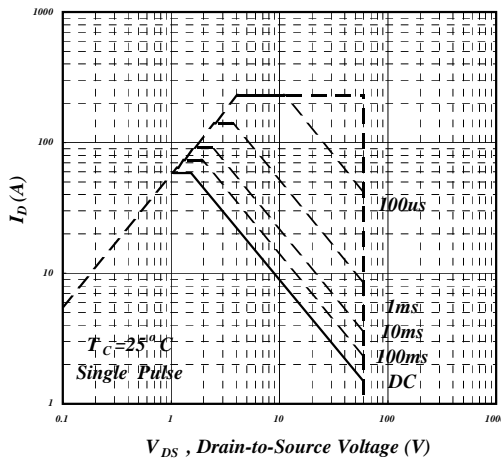


Fig 9. Maximum Safe Operating Area

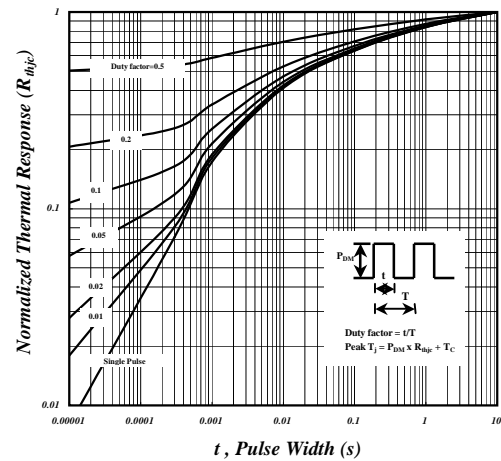


Fig 10. Effective Transient Thermal Impedance

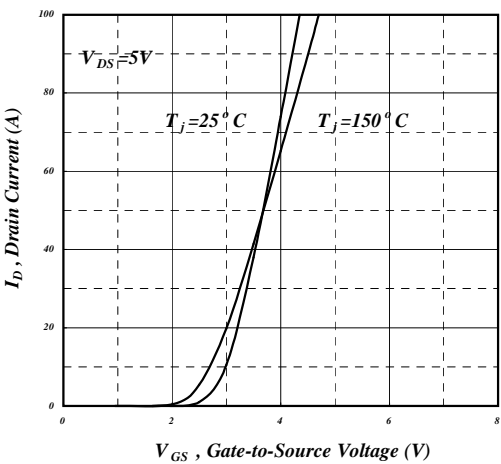


Fig 11. Transfer Characteristics

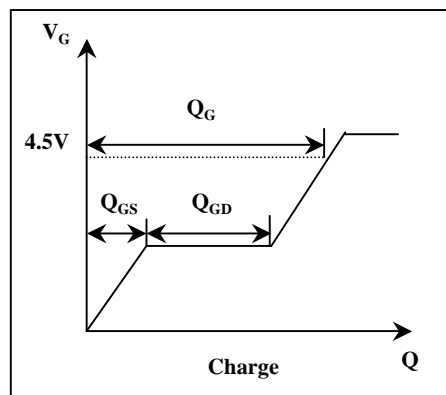
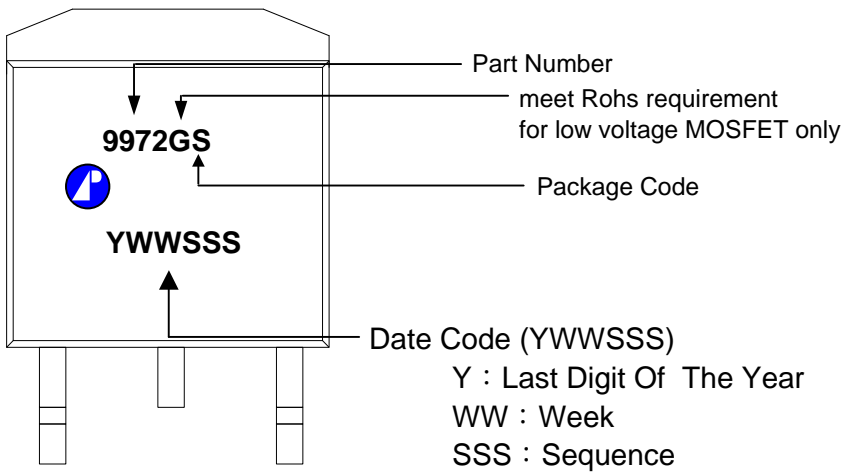


Fig 12. Gate Charge Waveform

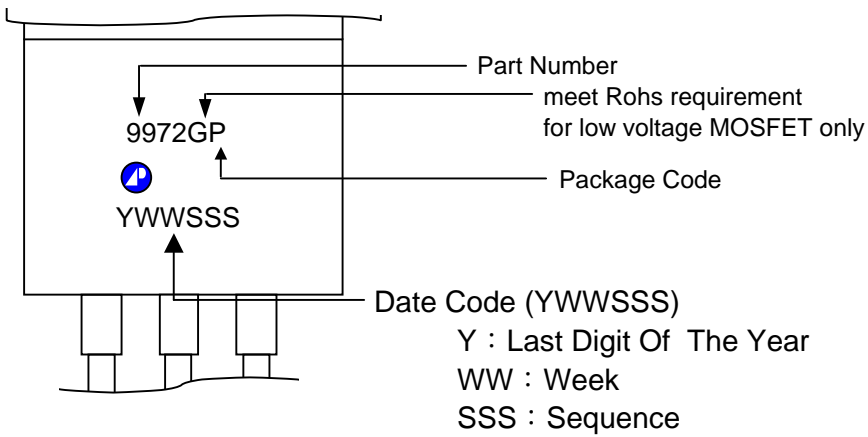


MARKING INFORMATION

TO-263

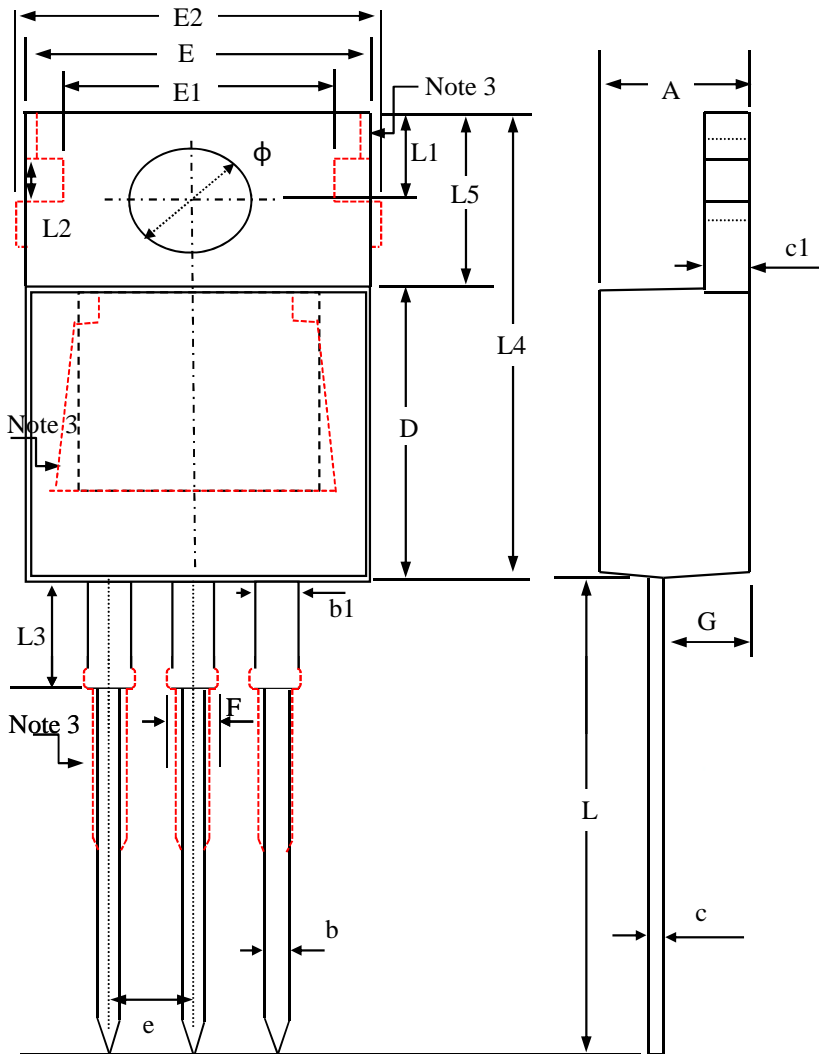


TO-220





Package Outline : TO-220



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.20	4.50	4.80
b	0.60	0.80	1.00
b1	1.10	1.38	1.80
c	0.30	0.48	0.65
c1	1.10	1.30	1.50
E	9.70	10.00	10.40
E1	7.40	8.30	9.20
e	2.54 (ref.)		
L	12.70	13.60	14.50
L1	2.50	2.75	3.00
L2	1.00	1.40	1.80
L3	2.60	3.35	4.10
L4	14.30	15.15	16.00
L5	6.00	6.40	6.80
ϕ	3.40	3.70	4.00
D	8.30	8.85	9.40
F	1.20	1.41	1.85
G	2.20	2.60	3.00
E2	—	—	11.50

Note:

1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.



TO-220 FOOTPRINT :

