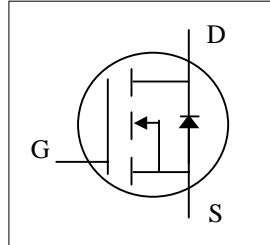




- ▼ 100% R_g & UIS Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

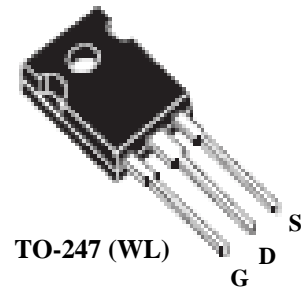


$V_{DS} @ T_{j,max.}$	700V
$R_{DS(ON)}$	0.19Ω
I_D^3	20A

Description

AP65SL190A series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-247 package is widely preferred for commercial-industrial applications. The device is suited for switch mode power supplies, DC-AC converters and high current high speed switching circuits.



Absolute Maximum Ratings @ $T_j = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	20	A
$I_D @ T_C = 100^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	12.3	A
I_{DM}	Pulsed Drain Current ¹	48	A
dv/dt	MOSFET dv/dt Ruggedness ($V_{DS} = 0 \dots 400V$)	50	V/ns
$P_D @ T_C = 25^\circ\text{C}$	Total Power Dissipation	147	W
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation	3.12	W
E_{AS}	Single Pulse Avalanche Energy ⁴	300	mJ
dv/dt	Peak Diode Recovery dv/dt ⁵	15	V/ns
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
R_{thj-c}	Maximum Thermal Resistance, Junction-case	0.85	$^\circ\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient	40	$^\circ\text{C}/\text{W}$



AP65SL190AWL

Electrical Characteristics @ $T_J=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=6.2A$	-	-	0.19	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	5	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=7.5A$	-	16	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=480V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_D=7.5A$	-	55	88	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=480V$	-	14	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	22	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=300V$	-	17	-	ns
t_r	Rise Time	$I_D=7.5A$	-	29	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	49	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	25	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	2200	3520	pF
C_{oss}	Output Capacitance	$V_{DS}=100V$	-	60	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	3	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	4.3	8.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=6.2A, V_{GS}=0V$	-	0.8	-	V
t_{rr}	Reverse Recovery Time	$I_S=20A, V_{GS}=0V$	-	420	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=50A/\mu s$	-	3.7	-	μC

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse test
3. Limited by max. junction temperature. Maximum duty cycle $D=0.75$
4. Starting $T_J=25^{\circ}\text{C}$, $V_{DD}=50V$, $L=150\text{mH}$, $R_G=25\Omega$
5. $I_{SD} \leq I_D$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^{\circ}\text{C}$

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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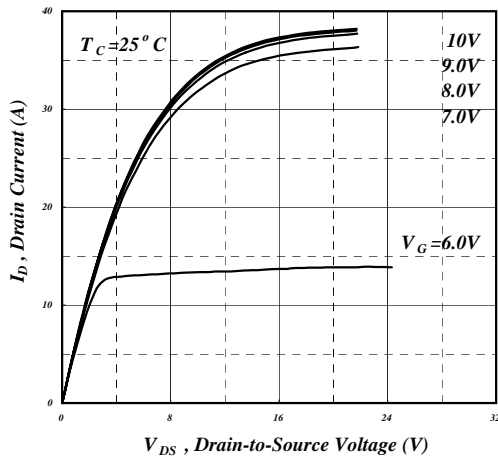


Fig 1. Typical Output Characteristics

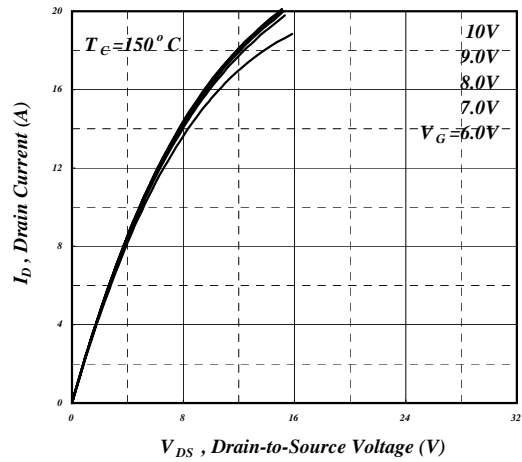


Fig 2. Typical Output Characteristics

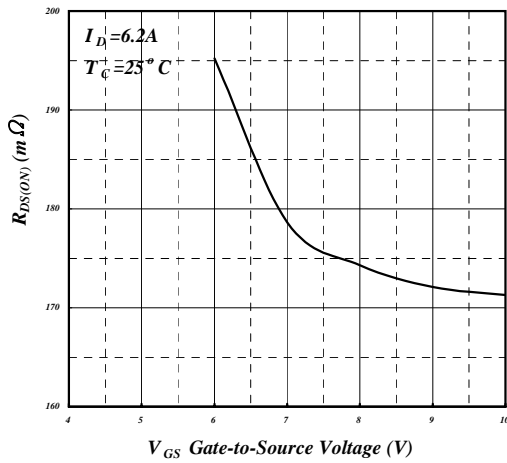


Fig 3. On-Resistance v.s. Gate Voltage

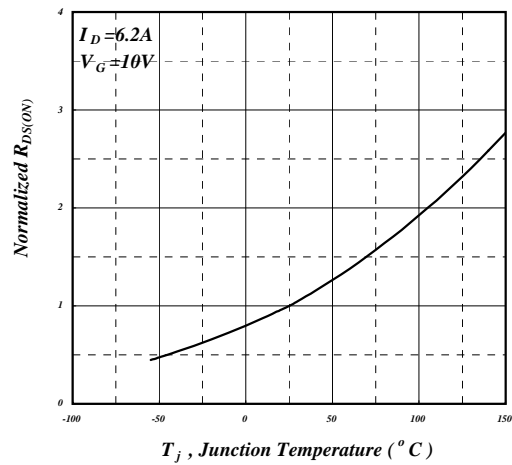


Fig 4. Normalized On-Resistance v.s. Junction Temperature

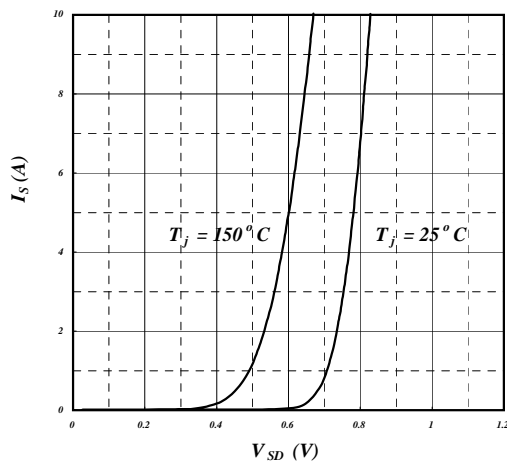


Fig 5. Forward Characteristic of Reverse Diode

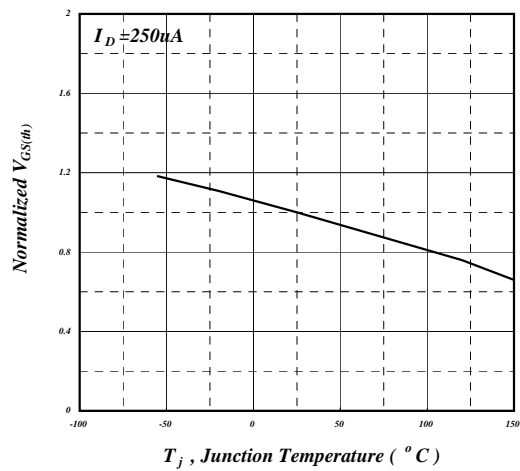


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

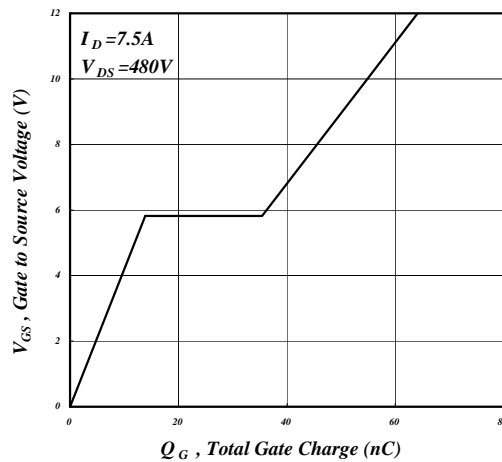


Fig 7. Gate Charge Characteristics

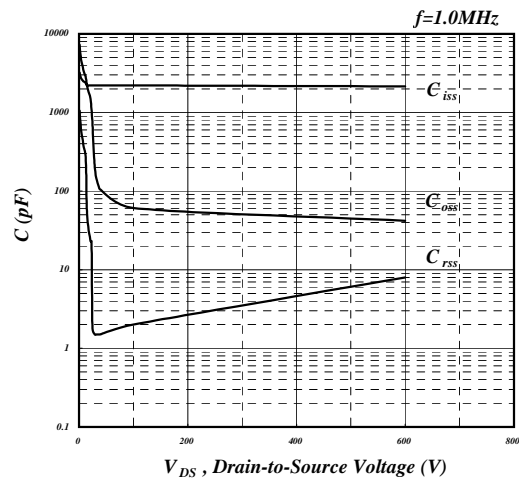


Fig 8. Typical Capacitance Characteristics

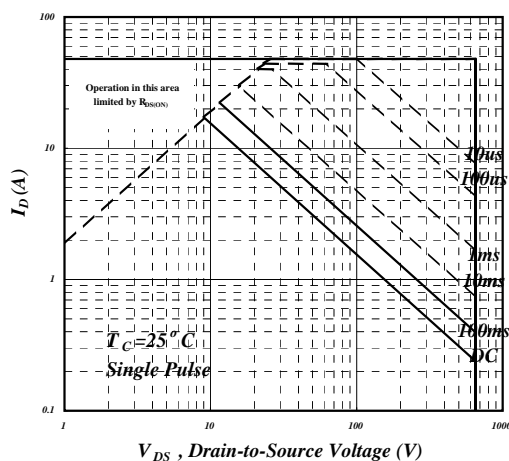


Fig 9. Maximum Safe Operating Area

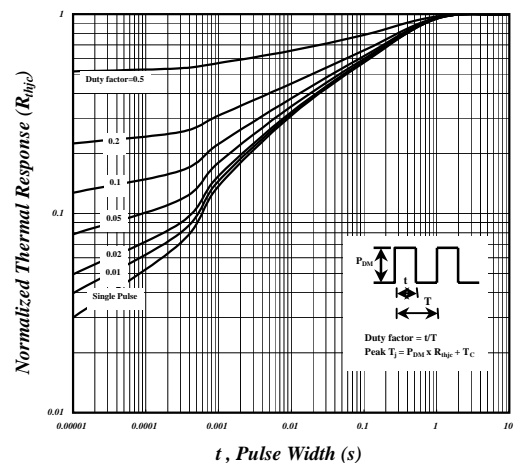


Fig 10. Effective Transient Thermal Impedance

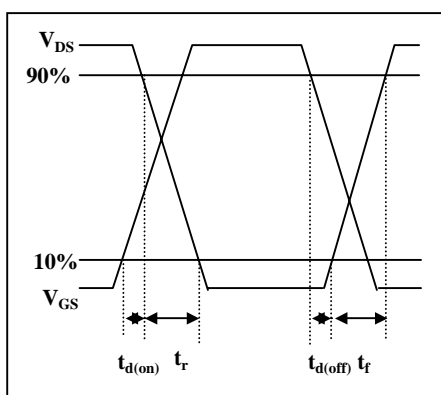


Fig 11. Switching Time Waveform

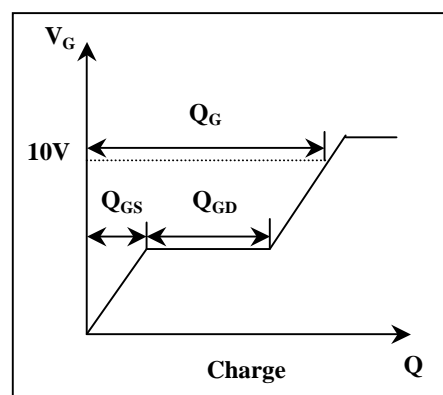


Fig 12. Gate Charge Waveform

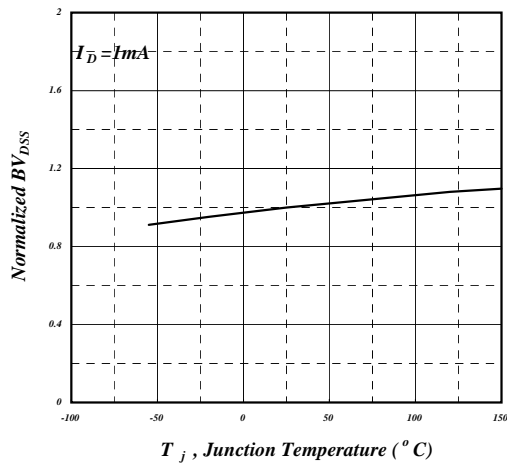


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

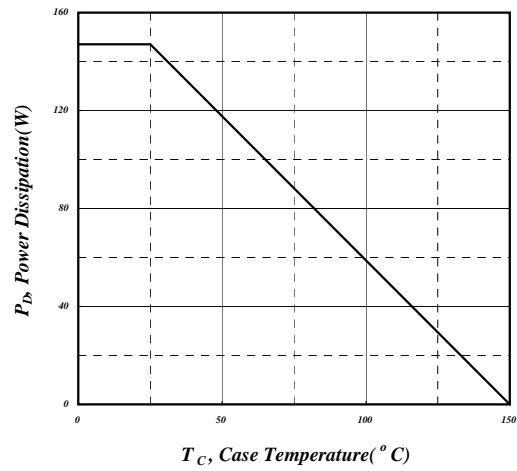


Fig 14. Total Power Dissipation

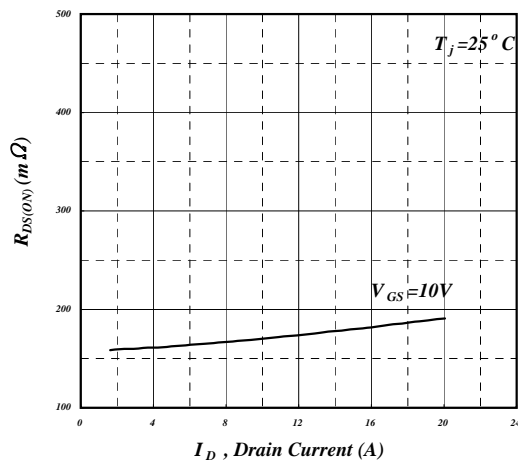


Fig 15. Typ. Drain-Source on State Resistance



AP65SL190AWL

MARKING INFORMATION

