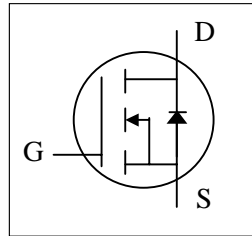
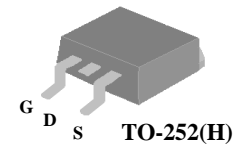




- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free



BV _{DSS}	60V
R _{DS(ON)}	3.5mΩ



Description

AP6NA3R5 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-252 package is widely preferred for all commercial-industrial surface mount applications using infrared reflow technique and suited for high current application due to the low connection resistance.

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	60	V
V _{GS}	Gate-Source Voltage	+20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Silicon Limited)	105	A
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Package Limited)	75	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	66	A
I _{DM}	Pulsed Drain Current ¹	360	A
P _D @T _C =25°C	Total Power Dissipation	69.4	W
P _D @T _A =25°C	Total Power Dissipation ³	2	W
E _{AS}	Single Pulse Avalanche Energy ⁶	173	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	1.8	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ³	62.5	°C/W



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Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =40A	-	-	3.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =40A	-	90	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =48V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	+0.1	uA
Q _g	Total Gate Charge ⁵	I _D =40A	-	62	99	nC
Q _{gs}	Gate-Source Charge ⁵	V _{DS} =30V	-	18	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge ⁵	V _{GS} =10V	-	17	-	nC
t _{d(on)}	Turn-on Delay Time ⁵	V _{DS} =30V	-	17	-	ns
t _r	Rise Time ⁵	I _D =40A	-	73	-	ns
t _{d(off)}	Turn-off Delay Time ⁵	R _G =6Ω	-	40	-	ns
t _f	Fall Time ⁵	V _{GS} =10V	-	90	-	ns
C _{iss}	Input Capacitance ⁵	V _{GS} =0V	-	3400	5440	pF
C _{oss}	Output Capacitance ⁵	V _{DS} =50V	-	560	-	pF
C _{rss}	Reverse Transfer Capacitance ⁵	f=1.0MHz	-	30	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =40A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time ⁵	I _S =40A, V _{GS} =0V	-	40	-	ns
Q _{rr}	Reverse Recovery Charge ⁵	di/dt=100A/μs	-	35	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board
- 4.Package limitation current is 75A .
- 5.Guaranteed by design.
- 6.Starting T_j=25°C , V_{DD}=30V , L=0.3mH , R_G=25Ω , V_{GS}=10V

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

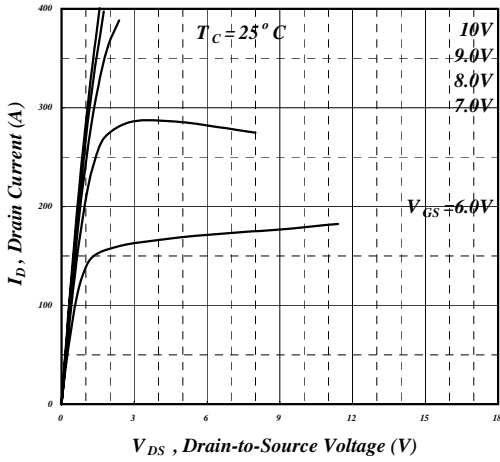


Fig 1. Typical Output Characteristics

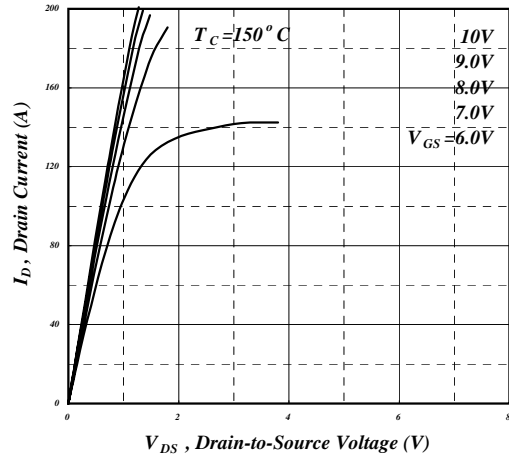


Fig 2. Typical Output Characteristics

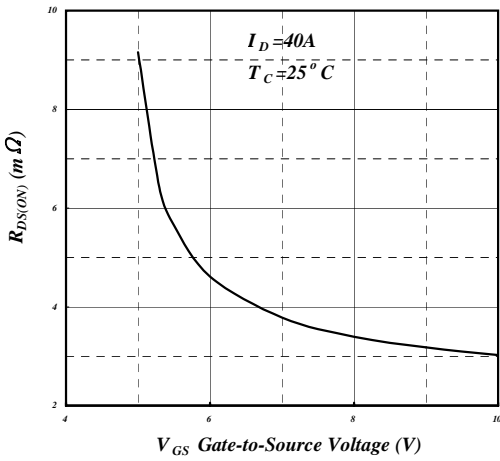


Fig 3. On-Resistance v.s. Gate Voltage

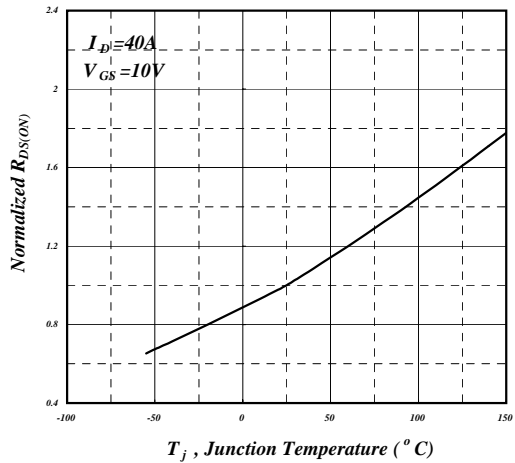


Fig 4. Normalized On-Resistance v.s. Junction Temperature

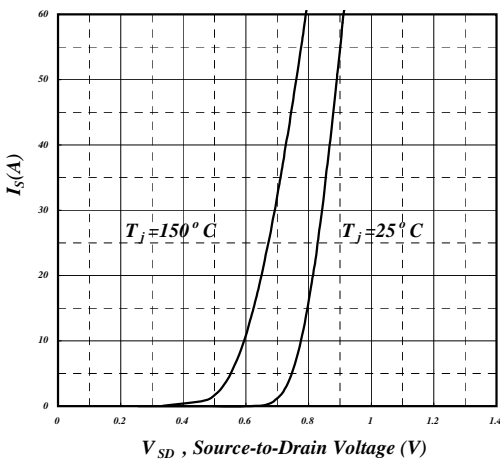


Fig 5. Forward Characteristic of Reverse Diode

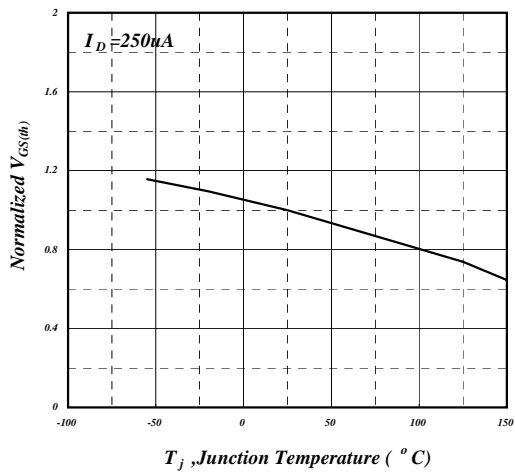


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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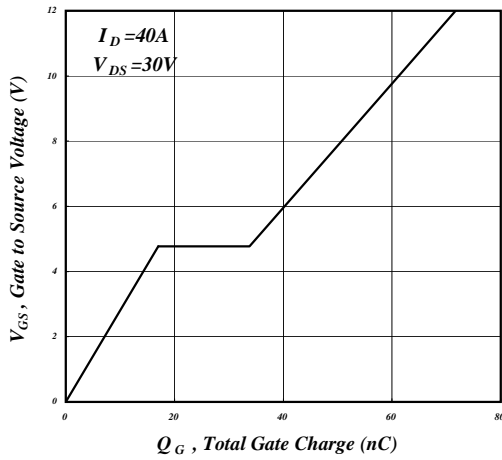


Fig 7. Gate Charge Characteristics

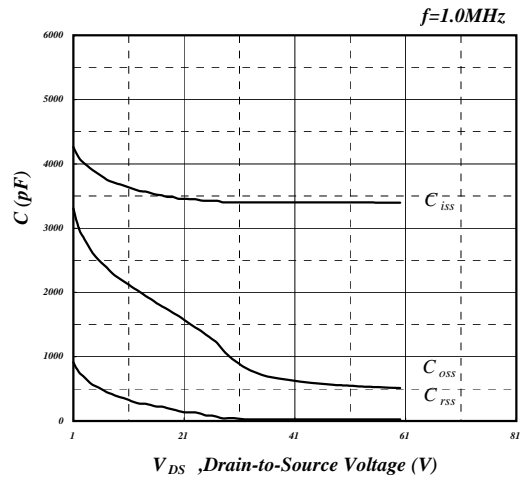


Fig 8. Typical Capacitance Characteristics

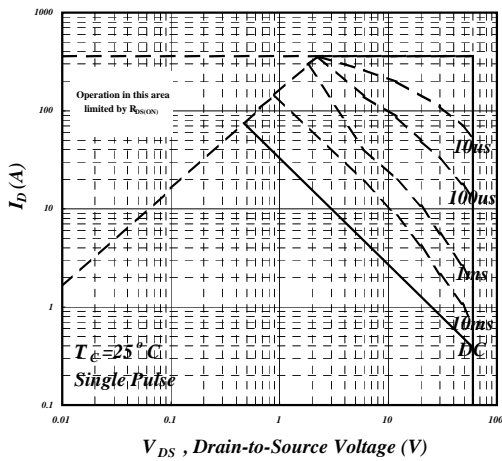


Fig 9. Maximum Safe Operating Area

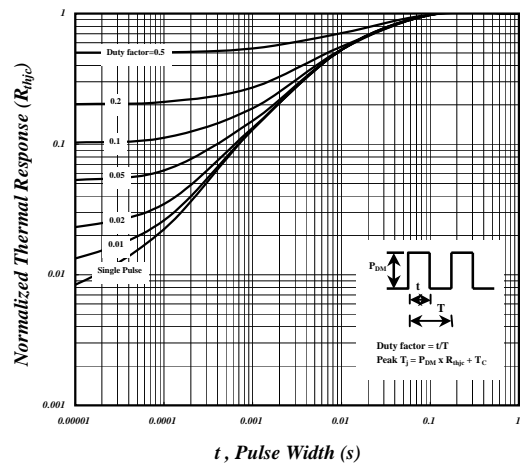


Fig 10. Effective Transient Thermal Impedance

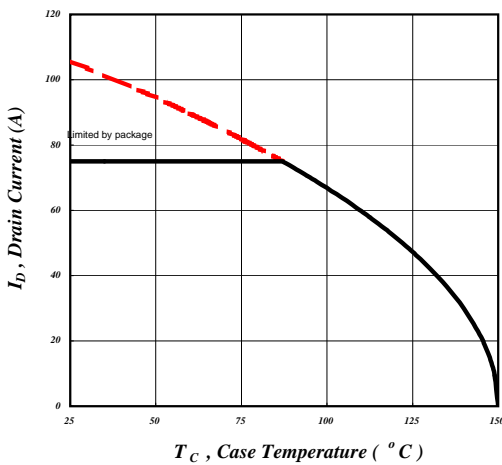


Fig 11. Drain Current v.s. Case Temperature

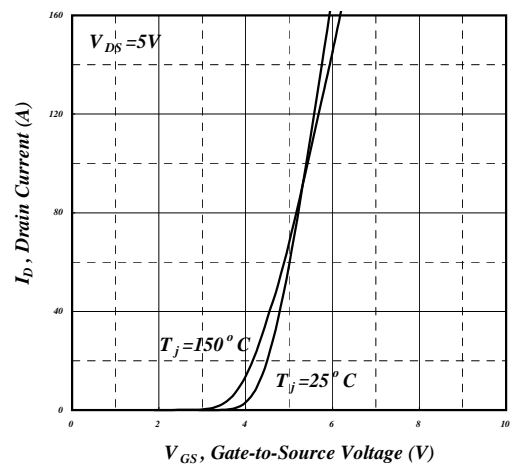


Fig 12. Transfer Characteristics

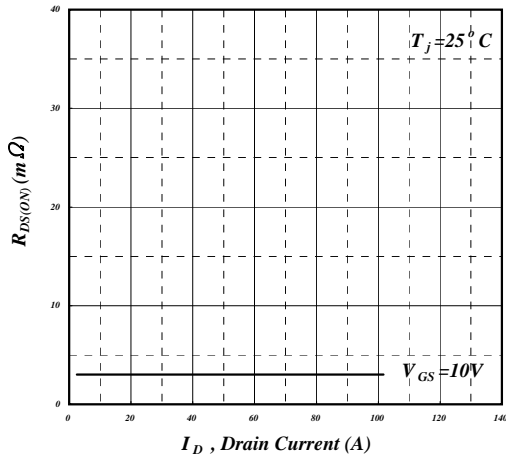


Fig 13. Typ. Drain-Source on State Resistance

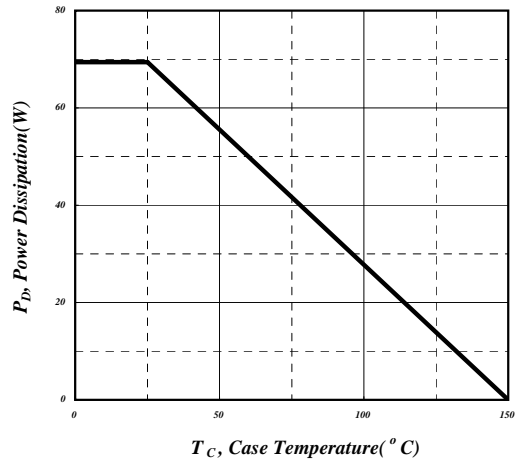


Fig 14. Total Power Dissipation

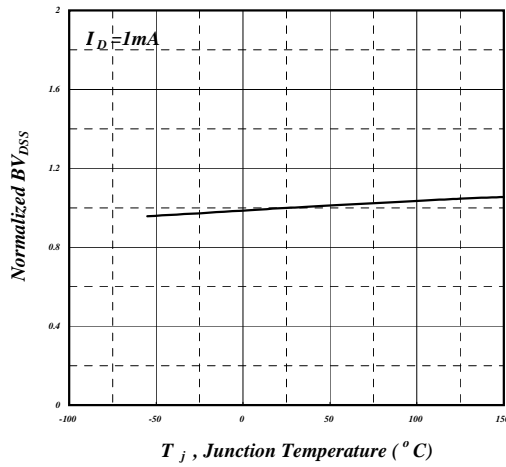


Fig 15. Normalized BV_{DSS} v.s. Junction Temperature



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MARKING INFORMATION

